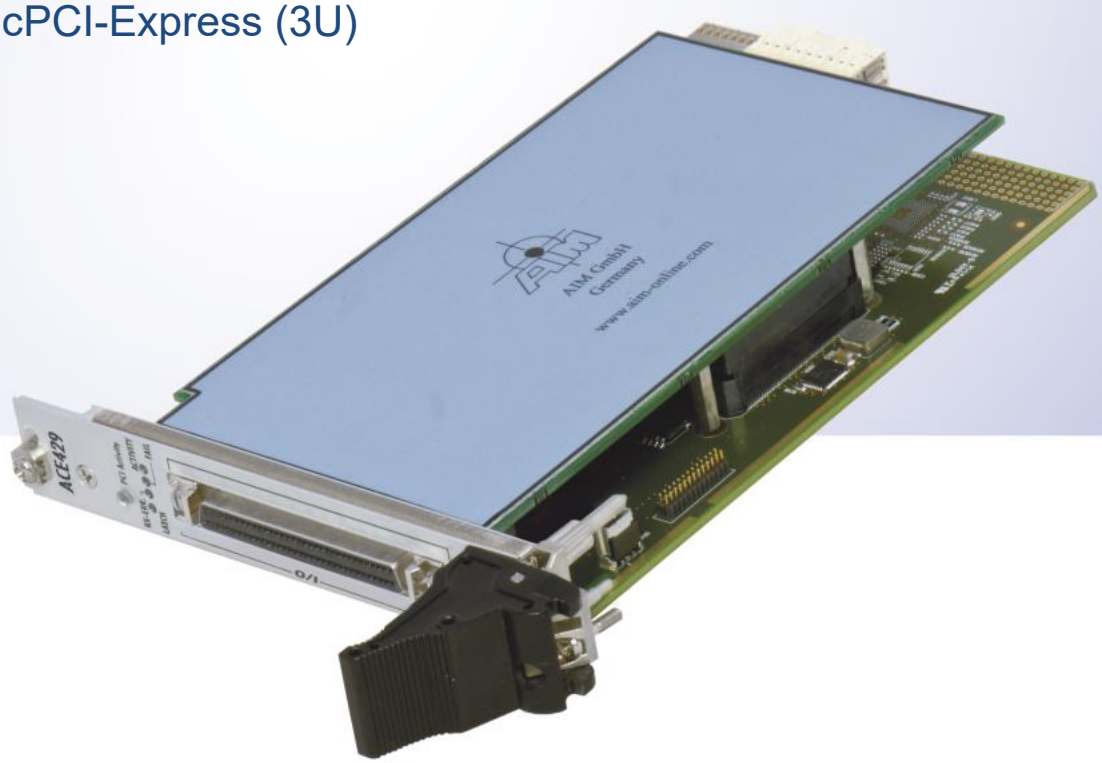
Avionics Databus Solutions

ACE429-3U

32 Channels ARINC429 Test & Simulation Module for PXI-Express / cPCI-Express (3U)



Hardware Manual

V01.01 Rev. A
April 2022

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DOCUMENT HISTORY

The following table defines the history of this document.

Version	Cover Date	Created by	Description
V01.00 Rev A	09.11.2016	S.Thota	First Released Version
V01.00 Rev B	06.07.2020	M.Schüssele	Formation, New title page picture
V01.01 Rev A	14.04.2022	M.Masood	Added more description into "Front Panel LEDs" chapter

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1 INTRODUCTION

1.1 General

This document comprises the Hardware User's Manual for the PXI-Express ACE429-3U-32, which implements 32 transmit and receive ARINC-429 channels, based on the PCI-Express communication standard. The document covers the hardware installation, board connections, technical data and a general description of the hardware architecture. For programming information please refer to the documents listed in the 'Applicable Documents' section.

The ACE429-3U-32 is a member of AIM's new family of Compact PCI-Express/PXI-Express (3U) modules for analysis, simulation, monitoring and testing of ARINC429 channels providing up to 32 channels on a 3U module form factor.
Each channel is software configurable in runtime as a fixed amplitude Transmitter or Receiver.

On the transmit channels, the ACE429-32 acts as an autonomously operating bus traffic simulator, supporting multiple modes of transmission sequencing. Full error injection capabilities are available, whereby the error injection is programmable individually for each channel and label. For special transmission operating modes the parity bit can be used alternatively as an additional data bit. The rise and fall time of the bus signals are individually programmable by software for each transmit channel.

For the receive channels, the ACE429-32 provides an advanced monitor and analyser function with unique on-board error detection, triggering and filtering capabilities. Monitor and analyser functions are available concurrently and independent from each other. The hardware architecture provides resources to guarantee that the performance of one function is not affected by the current load of the other function. The rise and fall times of the bus signals are individually programmable for each receive channel. To adapt to different transmit speeds, the transmission rate can be varied in discrete steps between approximately 90 and 120Kbits on the high speed bus and between 11.5 and 16.0Kbits on the low speed lines.

The hardware architecture provides ample resources (i.e. processing capability and memory) to guarantee, that all specified interface functions are available concurrently and to full performance specifications.

The advanced architecture uses a special processor for the ARINC-429 stream. A powerful PCI-Express Controller (1-lane up to 2.5 Gbit/s) and Memory Arbiter are implemented in a Field Programmable Gate Array (FPGA). This FPGA supports both, the interface to the application and driver software tasks running on the host computer and assists the communication for data transfer. This feature expands the capability of the ACE429-32 module to that of a high level instrument. To fulfil the real-time requirements of a typical avionic type data bus system, a high performance 32bit RISC processor (BIP) is implemented.

A free-wheeling IRIG-B Time code Encoder/Decoder is implemented on the ACE429-32 to satisfy the requirements of 'multi-channel time tag synchronization' on the system level. The IRIG-B compatible amplitude modulated sine wave output allows the synchronization of any external module implementing IRIG-B time stamping.
The module can be installed in standard cPCIe (3U) peripheral/hybrid slots and PXIe (3U) Peripheral/hybrid slots. If installed in a PXIe slot, 8 PXI Trigger I/O and a PXI System Reference Clock (10MHz) based time tag mode are supported.

1.2 How This Manual is organized

This ACE429-32 Hardware Manual is comprised of the following sections.

Section 1 Introduction - Contains an overview of this manual.
Section 2 Installation - Describes the steps required to install the ACE429-3U-32 device and connect the device to other external 429 interfaces, IRIG-B, and trigger out.
Section 3 Structure of the ACE429-32 - Describes the physical hardware Interfaces on the ACE429-32 using a block diagram and a description of each main component
Section 4 PXI-Express Instrumentation Bus - describes the PXI-Express Instrumentation Bus
Section 5 Technical Data - describes the technical specification of the ACE429-32.

1.3 Applicable Documents

The following documents shall be considered to be a part of this document to the extent that they are referenced herein. In the event of conflict between the documents referenced and the contents of this document, the contents of this document shall have precedence.

1.3.1 Industry Documents

[1] PXI Express Hardware Specification – Rev. 1.0 – Aug. 22, 2005
[2] PXI Hardware Specification – Rev. 2.2 – September 22, 2004

1.3.2 Product Specific Documents

[3] AIM - Reference Manual ACE429-32 Application Interface Library: Detailed description of the programming interface between the Host Carrier board and the onboard driver software.

2 INSTALLATION

2.1 Preparation and Precaution for Installation

The ACE429-32 features full PCI Plug and Play capability; therefore, there are no jumpers or switches on the board that require modification by the user in order to interface to the PCIe bus.

It is recommended to use a wrist strap for any installations. If there is no wrist wrap available, then touch a metal plate on your system to ground yourself and discharge any static electricity during the installation work.

2.2 Installation Instructions

The following instructions describe how to install the ACE429-32 module in your cPCIe/PXIe slots system. Please follow the instructions carefully, to avoid any damage on the device.

To Install the ACE429-32

1. Shutdown your system and all peripheral devices.
2. Unplug the power cord from the wall outlet. (Inserting or removing modules with power applied may result in damage to module devices).
3. Find a free peripheral/hybrid expansion slot in your system.
4. Remove the slot bracket from the slot you have chosen and put it aside.
5. Make sure the injector/ejector handle is in its downward position.
6. Align the ACE429 with the card guides on the top and bottom of the peripheral/hybrid expansion slot. Do not raise the injector/ejector handle as you insert.
7. Hold the handle as you slowly slide the module into the chassis until the handle catches on the injector/ejector rail.
8. Raise the injector/ejector handle until the module firmly seats into the backplane receptacle connectors. The front panel of the ACE429 should be even with the front of the chassis.
9. Secure the card to the cPCIe/PXIe chassis tightening the two bracket-retaining screws on the top and bottom of the front panel
10. Connect the system to the power source. Turn on the power of your system.

2.3 Connecting to other Devices

The connection to other devices is done via a SCSI-3 female connector.

The Front panel has 32 ARINC429 channels, IRIG IN/OUT and Trigger OUT.

The ACE429-3U-32 implementation has the capability to share the I/O- pins. This means each ARINC429 channel can be used as Transmit or Receive channel, but only one operation mode is possible at one time. The pinout is listed below.

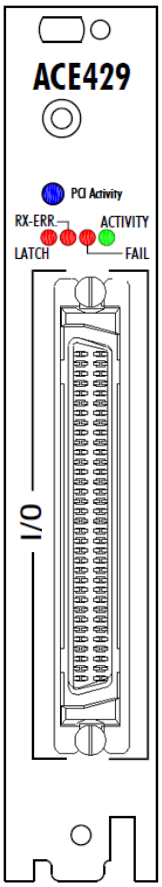

Figure 2-1: Front Panel view

2.3.1 ACE429-32 Front panel Connector Pinout

68 pin SCSI-3 female connector, Downward Compatibility Mode

Pin No.	Signal Description	Direction Type	Pin No.	Signal Description	Direction Type
1	TxRx_True_1	Bidir.	35	TxRx_Comp_1	Bidir.
2	TxRx_True_2	Bidir.	36	TxRx_Comp_2	Bidir.
3	TxRx_True_3	Bidir.	37	TxRx_Comp_3	Bidir.
4	TxRx_True_4	Bidir.	38	TxRx_Comp_4	Bidir.
5	TxRx_True_5	Bidir.	39	TxRx_Comp_5	Bidir.
6	TxRx_True_6	Bidir.	40	TxRx_Comp_6	Bidir.
7	TxRx_True_7	Bidir.	41	TxRx_Comp_7	Bidir.
8	TxRx_True_8	Bidir.	42	TxRx_Comp_8	Bidir.
9	TxRx_True_9	Bidir.	43	TxRx_Comp_9	Bidir.
10	TxRx_True_10	Bidir.	44	TxRx_Comp_10	Bidir.
11	TxRx_True_11	Bidir.	45	TxRx_Comp_11	Bidir.
12	TxRx_True_12	Bidir.	46	TxRx_Comp_12	Bidir.
13	TxRx_True_13	Bidir.	47	TxRx_Comp_13	Bidir.
14	TxRx_True_14	Bidir.	48	TxRx_Comp_14	Bidir.
15	TxRx_True_15	Bidir.	49	TxRx_Comp_15	Bidir.
16	TxRx_True_16	Bidir.	50	TxRx_Comp_16	Bidir.
17	TxRx_True_30	Bidir.	51	TxRx_Comp_30	Bidir.
18	TxRx_True_31	Bidir.	52	TxRx_Comp_31	Bidir.
19	TxRx_True_17	Bidir.	53	TxRx_Comp_17	Bidir.
20	TxRx_True_18	Bidir.	54	TxRx_Comp_18	Bidir.
21	TxRx_True_19	Bidir.	55	TxRx_Comp_19	Bidir.
22	TxRx_True_20	Bidir.	56	TxRx_Comp_20	Bidir.
23	TxRx_True_21	Bidir.	57	TxRx_Comp_21	Bidir.
24	TxRx_True_22	Bidir.	58	TxRx_Comp_22	Bidir.
25	TxRx_True_23	Bidir.	59	TxRx_Comp_23	Bidir.
26	TxRx_True_24	Bidir.	60	TxRx_Comp_24	Bidir.
27	TxRx_True_29	Bidir.	61	TxRx_Comp_29	Bidir.
28	GND	Pow.	62	TRIGGER_OUT	OUT
29	IRIG_IN	IN	63	IRIG_OUT	OUT
30	TxRx_True_25	Bidir.	64	TxRx_Comp_25	Bidir.
31	TxRx_True_26	Bidir.	65	TxRx_Comp_26	Bidir.
32	TxRx_True_27	Bidir.	66	TxRx_Comp_27	Bidir.
33	TxRx_True_28	Bidir.	67	TxRx_Comp_28	Bidir.
34	TxRx_True_32	Bidir.	68	TxRx_Comp_32	Bidir.

Table 2-1 : Pin assignment ACE429-32

2.4 Front Panel LEDs

Five subminiature LED's, as listed in Table 2-2, indicate the various conditions of the module at the front panel. The LED's are located in a quadruple LED-Array on the physical interface daughterboard. The first LED is used for indication of ARINC429 data streams of one or more channels. If data are transmitted, the green LED will be flashed. The second LED is used for board fail indication. If the board or any of the self-test routines have failed, the red LED will still be illuminated after power-up. After power-up, this LED is illuminated for app. 5 seconds. The third and fourth LED is used for error indication in a received data stream on any of the channels. If any error occurs, the third red LED will be flashed. The error event is stored and leads to an illumination of the fourth LED. During power-up or reset all LEDs are illuminated for self-test purposes.

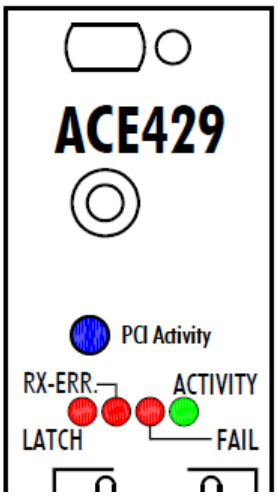

Figure 2-2: Status LED view

LED Name	Colour	Description
ACTIVITY	Green	LED flashes If data is transmitted on any channel.
FAIL	Red	LED illuminates if an error during the BIU self-test occurs.
RX-ERR	Red	LED flashes if an error on any channel is detected.
RX-ERR-LATCH	Red	LED illuminates if an error on any channel is detected (stored error).
PCI Activity	Blue	LED flashes if there is local (on board PCIe/PCI bus) activity

Table 2-2: Front Panel LED description

3 STRUCTURE OF THE ACE429-3U-32

The structure of the ACE429-3U-32 is shown in Figure 3-1. This card comprises the following main sections:

- PCI-Express bus and BIU-IO FPGA
- Global RAM
- BIU Processors Section (2-BIU's)
- Physical I/O Interface with 32 ARINC-429 channels and Trigger out
- IRIG- Time Code Proc. with free-wheeling function and Sine Wave Output
- Boot-Up Flash
- PXI Instrumentation Bus

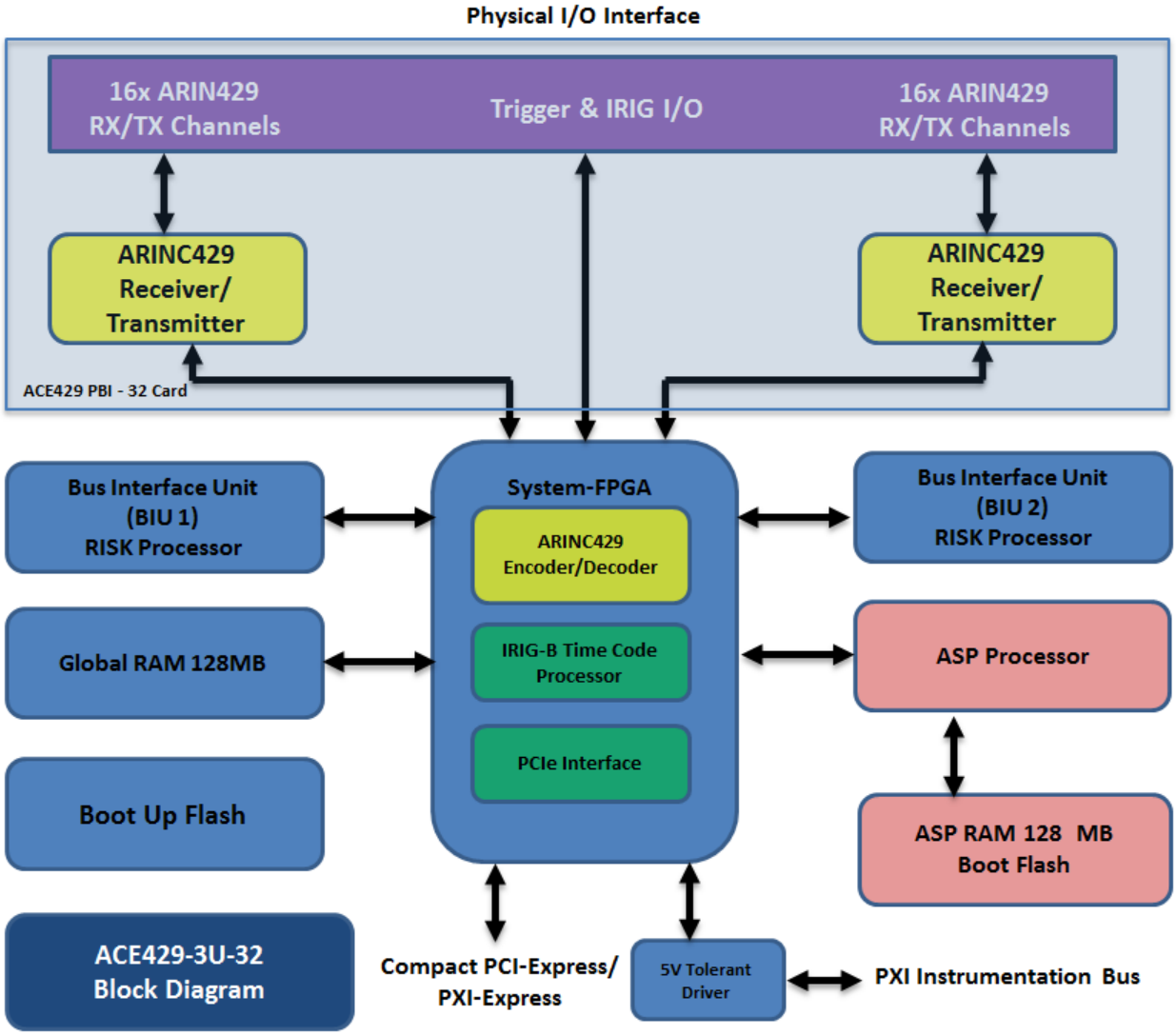

Figure 3-1: Block Diagram of ACE429-3U-32

3.1 PCI-Express bus and BIU-I/O FPGA

The new common FPGA architecture of AIM's PCI-Express family includes a complete PCI-Express bus logic (which is translated to a legacy PCI interface using an external bridge component) and the 2-BIU processors logic. This programmable device implements the following features:

- PCI Express 1.1 compliant bus interface
- Global RAM interface and arbitration
- Boot function
- SPI controller for update programming
- ARINC-429 Encoder
- ARINC-429 Decoder
- IRIG Encoder and decoder support
- External Trigger Output
- PXI Instrumentation Bus Capabilities

3.1.1 Global RAM Interface and Arbitration

The common FPGA implements a Global RAM arbiter, which controls the Global RAM access between both participants, the Host through the PCI-Express bus and the BIU processor.

3.1.2 Boot up

To provide maximum flexibility and upgradeability, the FPGA device and the processors are booted automatically from dedicated SPI-Flashes after power up.

3.2 Global RAM

The Global RAM is shared between both BIU processors (BIP) and the Host-Card Bus. The arbitration is handled by the common FPGA. It has access to the common Global RAM via a 32 bit wide data port.

3.3 BIU-Processors (BIP)

There are two physical BIU processors. Each BIP consists of an ultra-low power, high performance 32bit RISC processor.

3.4 ARINC-429 Encoder

The encoder converts the parallel data into a serial ARINC429 encoded data stream and appends the parity and the gap bits. The programmable frame-time between two labels can be set in the range from 0 up to 255 ARINC429 bits.

The encoder provides the following error injection capabilities:

- Gap Error (-1 bit)
- Bit count Error (+/- 1 bit)
- Coding Error (fixed at bit position 12)
- Parity Error (if no special transmission mode is chosen)

3.5 ARINC-429 Decoder

The decoder converts the serial received data stream into a parallel data double word and generates an additional 16 bit report for each received label. The decoder measures the gap time between two labels for gap error detection and bus load traffic detection.

The decoder provides the following error detection capabilities:

- Gap Error Detection
- Bit count Error Detection
- Coding Error Detection
- Parity Error Detection (if no special transmission mode is chosen)

3.6 External Trigger Output

One Trigger output is provided on ACE429-32 variant.

The Trigger output is TTL level compatible. Filter circuitry is provided at the trigger output to cover Electromagnetic Compatibility (EMC) aspects.

3.7 IRIG- and Time Code Section

The main functions of the Time Code Processor (TCP) are:

- IRIG-B compatible Time Code Decoder function
- Time code Encoder – IRIG-B compatible Time Encoder function

3.7.1 Time Code Encoder/Decoder

The generated time code signal is an IRIG-B compatible sinusoidal waveform. The time code information can be used for time-tagging and multi-channel synchronization. On the ACE429-32 a new generation IRIG-B section is implemented with a free-wheeling IRIG functionality. If no external IRIG signal is detected, the TCP switches automatically to the free-wheeling mode. Also, if an external IRIG-B signal is detected in free-wheeling mode, the Time tag is automatically synchronized to this external IRIG-B signal.

The time tag on the board is generated in the format explained in the following table:

Time Element	Number of bits
DAYS of Year	9
HOURS of Day	5
MINUTES of Hour	6
SECONDS of Minute	6
MICROSECONDS of Second	20
Summary	46 (6 Bytes, stored in two 32bit words)

Table 3-1: IRIG-B: Binary Coded Time Tag

3.7.2 Time Tag Methods

Besides the ARINC429 receive and transmit signals, the 68 pin SCSI-3 connector comprises one Trigger output signal as well as the IRIG-B- input and output as listed at all previous described Connector Pinout tables.

The IRIG-IN and IRIG-OUT signals shall be connected depending on the Time synchronisation method used as shown below.

1. **Single AIM-Module No External IRIG-B Source**
   No connection required
2. **Multiple AIM-Modules with No Common Synchronization Requirement**
   No connection required
3. **Single or Multiple AIM-Module(s) with External IRIG-B Source**
   Connect external IRIG-B source to IRIG-IN and GND of all modules
4. **Multiple AIM-Modules with No External IRIG-B Source Internally Synchronized.**
   Connect the IRIG-OUT signal and the GND of the module you have chosen as the time master to all IRIG-IN signals (including the time master).

3.8 PXIe / cPCIe - Connector Pin Assignment

PXIe introduces the usage of the I/O pins on XJ4 as legacy PXI triggers, Clock, Star and Local Bus signals. XJ3 carries the cPCIe reserved pins locations for the PCI-Express serial communication bus.

XJ4 Connector							
pin	Z	A	B	C	D	E	F
1	GND	GA4	GA3	GA2	GA1	GA0	GND
2	GND	5VAUX	GND	RSV	RSV	RSV	GND
3	GND	12V	12V	GND	GND	GND	GND
4	GND	GND	GND	3.3V	3.3V	3.3V	GND
5	GND	PXI_TRIG_3	PXI_TRIG_4	PXI_TRIG_5	GND	PXI_TRIG_6	GND
6	GND	PXI_TRIG_2	GND	RSV	PXI_STAR	PXI_CLK10	GND
7	GND	PXI_TRIG_1	PXI_TRIG_0	RSV	GND	PXI_TRIG_7	GND
8	GND	RSV	GND	RSV	PXI_LBL6	PXI_LBR6	GND

Table 3-2: PXIe XJ4 connector's pin-out

XJ3 Connector									
pin	A	B	ab	C	D	cd	E	F	ef
1	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND
2	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND
3	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND
4	RSV	PERST#	GND	RSV	RSV	GND	1refCLK+	1refCLK-	GND
5	1PETp0	1PETn0	GND	1PERp0	1PERn0	GND	RSV	RSV	GND
6	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND
7	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND
8	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND
9	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND
10	RSV	RSV	GND	RSV	RSV	GND	RSV	RSV	GND

Table 3-3: PXIe XJ3 connector's pin-out

RSV: Reserved Pin

3.9 General Purpose Discrete Inputs/Outputs (GPIO)

The ACE429-32 does not provide any General Purpose Discrete I/O's (GPIO's).

3.10 IRIG-B

See Chapter [3.7] for details.

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4 PXI-EXPRESS INSTRUMENTATION BUS

4.1 About the PXIe Standard

PCI Express was introduced to improve upon the PCI bus platform. The most notable PCIe advancement over PCI is its point-to-point bus topology. The shared bus used for PCI is replaced with a shared switch, which provides each device its own direct access to the bus. Unlike PCI, which divides bandwidth between all devices on the bus, PCIe provides each device with its own dedicated data pipeline. Because the cPCIe/PXIe backplane integrates PCI Express while still preserving compatibility with current PXI modules, users benefit from increasing bandwidth while maintaining backward compatibility with existing systems. PXIe specifies PXIe hybrid slots to deliver signals for both PCI and PCIe.

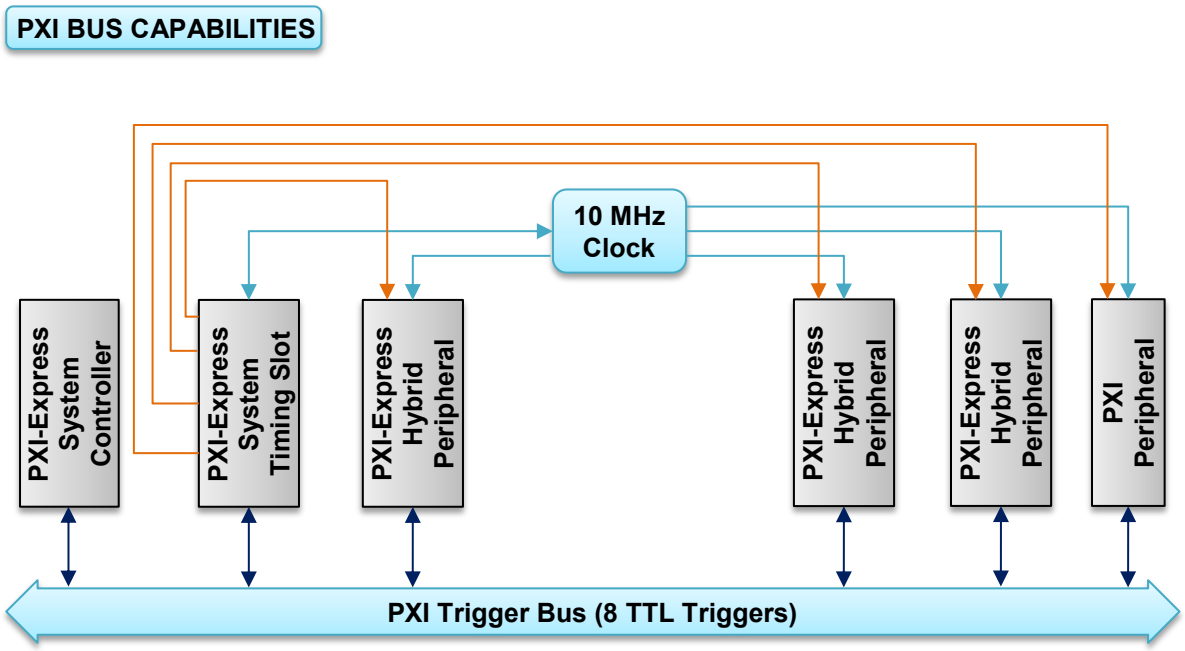

Figure 4-1: PXI architecture

PXIe combines industry-standard PC components, such as the PCI-Express bus, with advanced triggering and synchronization extensions on the backplane, backward compatible with the PXI triggering and synchronization bus.

The PXI-functions can be controlled via the API interface.

4.1.1 Backplane Trigger Lines

If the user requires a trigger bus, PXI triggers can be routed over the backplane instead of having to cable the cards together as one must do in a PC. The PXI backplane has eight dedicated trigger lines that are routed on the backplane to every slot, including the system controller slot. With these triggers, the user can achieve more sophisticated module synchronization, with features such as one module triggering another and asynchronous triggers. With asynchronous triggering, a module can be triggered by events occurring elsewhere. Finally, trigger signals can be routed into and out of the chassis with many of the newer controllers.

The ACE429-3U-32 card can route its Trigger INPUT and/or Trigger OUTPUT to the PXI backplane trigger lines, letting the user to deliver /receive trigger signals to/from other PXI cards present in the system (a Trigger Controller, another AIM PXI-capable product).

Please NOTE: ***The PXI triggers on the backplane are ACTIVE LOW.***
For electrical specification please refer to reference [1] and [2].

4.1.2 System Reference Clock (10MHz)

The PXI backplane has a built-in, dedicated 10 MHz system clock.
This very high quality clock, with low skew signals between each slot, is used for synchronizing modules. When boards are synchronized in an industrial PC, or any other system for that matter, they must be cabled together with a proprietary trigger bus and timing sources on the boards are used to time and trigger the boards. Because the quality and precision of the clock depends on the individual device, some are more or less precise than the industrial PC chassis clock. However, because the clock signals are routed among boards, they have a higher skew – typically nanoseconds versus picoseconds – than the chassis clock and the signals are not shielded. The PXI system clock is able to maintain its quality by using a low-skew, fan-out buffer chip that essentially provides a unique clock for every slot. Furthermore, because the clock lines are built into the backplane, the lines are better shielded than external lines.

The ACE429-3U-32 card can be set to deliver the PXI 10 MHz System Clock to its internal TIME TAG generation circuitry. The IRIG decoder will then work in Free-Wheeling mode but synchronous to the PXI 10 MHz clock. It is possible to maintain the synchronization among more AIM PXI-capable cards on the same backplane using the TIME TAG reset feature (see next paragraph).

Please NOTE: ***For electrical specification please refer to reference [1] and [2].***

4.1.3 Star Trigger

The PXI backplane defines specific layout requirements so that the star trigger lines provide matched propagation time from the star trigger slot to each module for very precise trigger relationships between each module. The star trigger is a high-performance trigger signal, which can synchronize all of the modules in a chassis. You can also synchronize the modules using the normal PXI trigger bus, but the star trigger offers increased performance. Specifically, the star trigger provides a skew of less than 1 ns and a delay between the star trigger slot and each peripheral slot of no more than 5 ns.

To use the star trigger, a module with the ability to generate the star trigger must be placed in Slot 2 of the chassis. Slot 2 is dedicated for the star trigger controller (although any standard module placed in Slot 2 will function normally in an application where star triggering is not required). Receiving modules must also be designed to be able to accept the star trigger.

The standard PXI trigger bus can perform the same functionality with a trigger signal from any chassis slot, but with less precise timing.

The ACE429-3U-32 card can use the PXI STAR input signal to perform a TTAG reset (clear) to DAY 1. This TTAG reset to DAY 1 will work if the IRIG circuitry is running in Free-Wheeling mode:

- External IRIG signal selected, but no signal connected
- PXI 10MHz System Clock connected to the IRIG decoder

The TTAG clear to DAY 1 can be either triggered via PXI Star signal or via PXI Trigger Input 0.

Please NOTE: ***The PXI Star signal on the backplane is ACTIVE LOW. For electrical specification please refer to reference [1] and [2]***

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5 TECHNICAL DATA

PXI-Express / Compact PCI-Express bus:

Compatible with PCI-Express Standard (Release 1.1)
3.3V PCI-Express - 1xlane PCI-Express bus operation 2.5 Gbit/s
PXI-Express / Compact PCI-Express Hybrid/Peripheral slot compatibility

Memory:

Fast Industrial DDR2-RAM
128 MByte memory size
16 bit wide organized
Shared between BIU-processor and PCI Express bus

BIU-Section: (2 BIUs are Present)

Low power, high performance 32bit RISC Processor;
Core voltage 1.0V,
Core speed 400 MHz,
External bus speed 100 MHz

Encoder:

Programmable Bitrate High / Low Speed (100 / 12.5 Kbit/sec)
Programmable gap between two labels are in the range from 0 up to 255 ARINC 429 bits.
ARINC429-Label Bit-32 programmable as Parity or additional Data Bit

Error injection capabilities:

Gap Error	(-1 bit)
Bit count Error	(+/- 1 bit)
Coding Error	(fixed at bit position 12)
Parity Error	(if no special transmission mode is chosen)

Decoder:

Valid Receive Range Transmission speed select +/- approx. 10%
ARINC429-Label Bit-32 programmable as Parity or additional Data Bit Measurement of gap between two labels in the range from 0.0 to 58.75 bits with 0.25bit resolution.

Error detection capabilities:
Gap Error Detection
Bit count Error Detection
Coding Error Detection
Parity Error Detection (if no special transmission mode is chosen)

Time Tagging:

IRIG B Time Tag:
For absolute time tagging, a special time code processor implements an IRIG-B encoder/decoder. If no external IRIG-B source is available a time code in IRIG B format is generated and can be used to synchronize multiple boards or modules.

Decoder:

Format:	IRIG-B-122
Resolution:	1 µs
Width:	1 Year (46 Bit)
Signal Waveform:	Amplitude modulated sine wave or square wave
Modulation Ratio:	3:1 to 6:1
Input Amplitude:	0.6Vp-p to 5Vp-p
Input Impedance:	~ 10k ohm
Coupling:	AC coupled
Time Jitter:	+/- 5µs (depending on the input signal quality)
Lock time:	< 5s

Free-wheeling accuracy after 10 Minutes < 1ppm (assuming input signal accuracy better than 50ppm)

Encoder:

Format:	IRIG-B-122
Absolute Accuracy:	+/-25ppm (standard Oscillator)
Signal Waveform:	Amplitude modulated sine wave
Output Amplitude:	~ 4.5 Vp-p, High voltage level
Output Impedance:	~ 51 ohm
Coupling:	AC coupled
Modulation Ratio:	~ 3:1
Carrier Frequency:	1 kHz +/-50ppm

Connectors:

Rear Connector XJ3: High-Speed Advanced Differential Fabric (ADF) connector (30 contact pairs, 30 ground contacts, female connector) for PCIe connection
Rear Connector XJ4: shielded 5-row by 8-column (40 pins) Hard Metric (eHM) female connector for power supply rails (+3.3V, +12V) and for PXI bus capabilities
Front Connector: 68 pol. standard female SCSI-3

Line Transmitter:

Transmitter channel Output Impedance 75 Ω
Channel 1-32 are fixed output amplitude of typically ± 10 V
High / Low Speed: Rise and fall time automatically switched via Analogue Switches to meet the requirement for High / Low

Speed operation

Line Receiver:

Input Impedance A to B: typ. 50 kΩ
Input Impedance A/B to GND: typ. 25 kΩ

Trigger Out:

Output with TTL Level; with high speed EMV varistor,
High Pulse width strobe, 500ns duration.

PXI Trigger Bus / STAR / Clock:

All PXI Inputs are TTL Level compatible
Active LOW (falling edge) Trigger Input (also Star) and Trigger Outputs
Pulse-width multiple of 100ns

Supply Voltage:

Standard PC – Supply +3.3V, +12.0V

Dimensions:

100.00 x 160.00 mm

Power Consumption:

PCIe Voltages	Idle	Operating HS	Operating LS(1)	Operating LS(2)
+3.3V	3.84	4.55	4.55	8.45
+12V	2.04	2.28	2.28	2.28
Overall Power	5.88	6.83	6.83	10.73

(1) High Speed (HS) 100 kHz; no load; 100 % Duty Cycle
(2) Low Speed (LS1) 12, 5 kHz; no load; 100 % Duty Cycle
(3) Low Speed (LS2) 12, 5 kHz; worst case load (400 Ohm || 30 nF); 100 % Duty Cycle

Temperature:

Standard Operating	0 to +50°C
Extended Temperature (on request)	-15 to +60°C
Storage	-40 to +85°C

Humidity:

0% to 95% non-condensing

Weight:

~ 200g for the ACE429-32

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6 NOTES

6.1 Acronyms

ADC	Analog to Digital Converter
ALBI	ASP Local Bus Interface
API	Application Programming Interface
ARM	Advanced RISC Machine
ARINC	AERONAUTICAL RADIO, INC
ASP	Application Support Processor
BIP	Bus Interface Processor
BIU	Bus Interface Unit
BSP	Board Software Package
CPCI	Compact PCI
cPCIe	Compact PCI express
DAC	Digital to Analog Converter
DRAM	Dynamic Random Access Memory
EEPROM	Electrically Erasable and Programmable Read Only Memory
EMC	Electromagnetic Compatibility
FLASH	Page oriented electrical erasable and programmable memory
FPGA	Field Programmable Gate Array
GND	Ground
IRIG B	Inter Range Instrumentations Group Time code Format Type B
I/O	Input / Output
JTAG	Joint Test Action Group (IEEE 1149.1 Boundary Scan)
LCA	Logic Cell Array (Field Programmable Logic)
N/A	Not Applicable
NC	Not Connected
PC	Personal Computer
PCB	Printed Circuit Board
PROM	Programmable Read Only Memory
PCI	Peripheral component interconnect
PCIe	Peripheral component interconnect Express
PBI	Physical Bus Interface (Daughterboard)
PXI	PCI eXtensions for Instrumentation
PXIe	PCI express eXtensions for Instrumentation
RISC	Reduced Instruction Set Computer
RAM	Random Access Memory
SIMM	Single Inline Memory Module
SRAM	Static Random Access Memory
SSRAM	Synchronous Static Random Access Memory
SDRAM	Synchronous Dynamic RAM
SW	Software
TAP	Test Access Port (for JTAG)
TCP	Time Code Processor
UART	Universal Asynchronous Receiver and Transmitter

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7 CERTIFICATE OF VOLATILITY

Model: ACE429-32-3U

Part-Number: 127C6-0101

Manufacturer: AIM GmbH
Sasbacher Str. 2
D-79111 Freiburg
Germany

Volatile Memory				
Does the item contain volatile memory (i.e., memory whose contents are lost when power is removed)? ☒ Yes ☐ No				
Description of used volatile memory:				
Type: DDR2-RAM DDR2-RAM	Size: 128 Mbyte 128 MByte	User Modifiable: ☒ Yes ☒ Yes	Function: Buffers, Global RAM ASP Local RAM	Process to Sanitize: Power off / on Cycle Power off / on Cycle
Non-Volatile Memory				
Does the item contain non-volatile memory (i.e., memory whose contents are retained when power is removed)? ☒ Yes ☐ No				
Description of used non-volatile memory:				
Type: Serial SPI-Flash	Size: 64 Mbit	User Modifiable: ☒ No	Function: FPGA Boot	Process to Sanitize: Erase
Type: Serial SPI-Flash Serial SPI-Flash Serial SPI-Flash	Size: 8 Mbit 8 Mbit 8 Mbit	User Modifiable: ☒ No ☒ No ☒ No	Function: BIU1 CPU Boot BIU2 CPU Boot ASP CPU Boot	Process to Sanitize: Erase Erase Erase
Type: NAND-Flash	Size: 256 MByte	User Modifiable: ☐ Yes ☒ No	Function: ASP Personalization	Process to Sanitize: Erase
Media				
Does the item contain media storage capability (i.e., removable or non-removable disk drives, tape drives, memory cards, etc.)? ☐ Yes ☒ No				
Description of used media storage:				
Type: -None-	Size: -	User Modifiable: ☐ Yes ☐ No	Function: -	Process to Sanitize: -
Additional Information:				
Test Engineer				
Name: Saikanth Thota	Title: Hardware Engineer		Date of Certification: 09.11.2016	

All operating Data for handling the I/O Protocol will be stored in volatile memory only. No Transfer data is stored in Non-Volatile Memory. The Non-Volatile Memory only contains production relevant data for board personalization, FPGA Logic or Firmware Code for the on board Microcontroller.