Manufacturer: NI

Board Assembly Part Numbers (Refer to Procedure 1 for identification procedure)**:**

Part Number and Revision	Description
149288A-01L or later	cRIO-9053
149288A-02L or later	cRIO-9054
149288A-03L or later	cRIO-9055
149288A-13L or later	cRIO-9055 (Conformal-coated)
146494C-01L or later	cRIO-9056
146494C-02L or later	cRIO-9057
146494C-03L or later	cRIO-9058
146494C-13L or later	cRIO-9058 (Conformal-coated)

Volatile Memory

Target Data	*Type*	*Size*	*Battery Backup*	*User[1] Accessible*	*System Accessible*	*Sanitization Procedure*
System memory	SDRAM	1 GB (cRIO-9053,9056) 2 GB (cRIO-9054,9055,9057,9058)	No	Yes	Yes	Cycle Power
LabVIEW and user data	FPGA	Xilinx XC7A50T (cRIO-9053) Xilinx XC7A75T (cRIO-9056) Xilinx XC7A100T (cRIO-9054,9055,9057,9058)	No	Yes	Yes	Cycle Power
CPLD memory	CPLD	Lattice LCMXO2-1200HC	No	No	Yes	Cycle Power
Real-time clock	SoC RTC RAM	242 Bytes	Yes	Yes	Yes	Procedure 2
ASIC firmware	RAM	8 MB	No	No	Yes	Cycle Power

Non-Volatile Memory (*incl. Media Storage*)

Target Data	*Type*	*Size*	*Battery Backup*	*User Accessible*	*System Accessible*	*Sanitization Procedure*
Primary storage	Disk-on-Chip	4 GB	No			
• Safe mode				No	Yes	None
• Operating system				No	Yes	Procedure 3
• User data				Yes	Yes	Procedure 3
FPGA storage	Flash	4 MB	No			
• FPGA firmware				No	Yes	None
• User FPGA VI bitstream				Yes	Yes	Procedure 4
General logic	CPLD	Lattice LCMXO2-1200HC	No	No	Yes	None
ASIC firmware	Flash	1 MB	No	No	Yes	None
Ethernet firmware	NVM	512 KB	No	No	Yes	None
Ethernet firmware	NVM	512 KB (cRIO-9054,9055,9057,9058 only)	No	No	Yes	None
DDR SPD EEPROM	EEPROM	256 Bytes	No	No	Yes	None
BIOS firmware	Flash	8 MB	No	No	Yes	None

[1] Refer to *Terms and Definitions* section for clarification of *User* and *System Accessible*

Procedures

Procedure 1 – Board Assembly Part Number identification:
To determine the Board Assembly Part Number and Revision, check the top left corner of the white label on the bottom of the module. The Assembly Part Number should be formatted as 14####A-##L, where 'A' is the letter revision of the assembly (e.g. A, B, C…)and "#" is the number that identifies the model from the Board Assembly Part Number table .

Procedure 2 – SoC RTC RAM (Real-Time Clock Data):
The battery-backed Real-Time Clock data can be cleared from the SoC RTC RAM using the CMOS reset button.
To clear the Real-Time Clock data, perform the following steps:

1. Disconnect power from the cRIO controller.
2. Locate the CMOS reset button in the center of the cRIO backplane.
3. Press the CMOS reset button and hold it for 1 second.

Procedure 3 – Primary Storage Disk-on-Chip (OS and User Data):
The Primary Storage DoC can be reformatted to clear the OS and User Data areas. The format operation is a "quick format" that re-initializes the file table, thereby making the existing files inaccessible. Format the drive for this NI Linux Real-Time target by performing one of the following steps:

1. Right-click the controller in MAX and click on "Format Drive".
2. Issue the nisystemformat command via a serial console local connection or SSH remote connection. Visit ni.com/info and enter the info code *format* for details.
3. Write a LabVIEW program that invokes the Format VI of the System Configuration API for the controller

Procedure 4 – FPGA Storage Flash (User FPGA Bitstream):
The User FPGA Bitstream in the FPGA Storage Flash can be cleared using NI-RIO Device Setup. To clear the bitstream from the flash, perform the following steps:

1. Add the cRIO target to your LabVIEW project by right-clicking on the project and selecting "New » Targets and Devices" and selecting your cRIO.
2. Right-click on the FPGA project item and select RIO Device Setup.
3. In the *Advanced* section, select *Erase Bitfile on Flash*.

Terms and Definitions

Cycle Power:
The process of completely removing power from the device and its components and allowing for adequate discharge. This process includes a complete shutdown of the PC and/or chassis containing the device; a reboot is not sufficient for the completion of this process.

Volatile Memory:
Requires power to maintain the stored information. When power is removed from this memory, its contents are lost. This type of memory typically contains application specific data such as capture waveforms.

Non-Volatile Memory:
Power is not required to maintain the stored information. Device retains its contents when power is removed.
This type of memory typically contains information necessary to boot, configure, or calibrate the product or may include device power up states.

User Accessible:
The component is read and/or write addressable such that a user can store arbitrary information to the component from the host using a publicly distributed NI tool, such as a Driver API, the System Configuration API, or MAX.

System Accessible:
The component is read and/or write addressable from the host without the need to physically alter the product.

Clearing:
Per *NIST Special Publication 800-88 Revision 1*, “clearing” is a logical technique to sanitize data in all User Accessible storage locations for protection against simple non-invasive data recovery techniques using the same interface available to the user; typically applied through the standard read and write commands to the storage device.

Sanitization:
Per *NIST Special Publication 800-88 Revision 1*, “sanitization” is a process to render access to “Target Data” on the media infeasible for a given level of effort. In this document, clearing is the degree of sanitization described.