NI-5731/5732/5733 User Guide and Specifications

The NI-5731/5732/5733/5734 is a family of high-speed digitizer adapter modules designed to work in conjunction with your NI FlexRIO™ FPGA module. This document contains signal information and specifications for the NI-5731/5732/5733/5734R, which is composed of an NI FlexRIO FPGA module and the NI-5731/5732/5733/5734. This document also contains tutorial sections that demonstrate how to acquire data using a LabVIEW FPGA example VI and how to create and run your own LabVIEW project with the NI-5731/5732/5733/5734R.

Note The NI-5734 information in this document is out of date. Refer to `ni.com/docs` for updated NI-5734 product documentation.

Note *NI-5731/5732/5733/5734R* refers to the combination of your NI-5731/5732/5733/5734 adapter module and your NI FlexRIO FPGA module. *NI-5731/5732/5733/5734* refers to your NI-5731/5732/5733/5734 adapter module only.

A description of each of the NI-5731/5732/5733/5734 devices is given below:

- **NI-5731**—2 analog input, 12-bit, 40 MS/s digitizer
- **NI-5732**—2 analog input, 14-bit, 80 MS/s digitizer
- **NI-5733**—2 analog input, 16-bit, 120 MS/s digitizer
- **NI-5734**—4 analog input, 16-bit, 120 MS/s digitizer

Contents

Note Before configuring your NI-5731/5732/5733/5734R, you must install the appropriate software and hardware. Refer to the *NI FlexRIO FPGA Module Installation Guide and Specifications* for installation instructions. Figure 1 shows an example of a properly connected NI FlexRIO device.

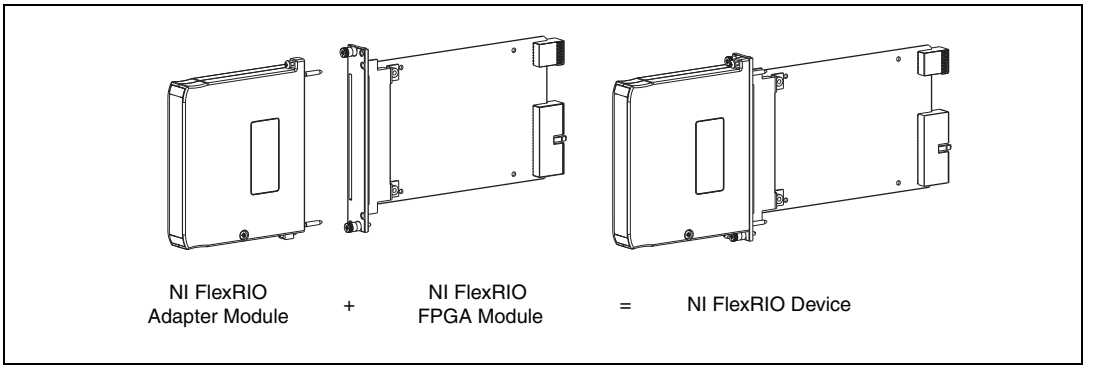


Figure 1. NI FlexRIO Device

Electromagnetic Compatibility Guidelines

This product was tested and complies with the regulatory requirements and limits for electromagnetic compatibility (EMC) as stated in the product specifications. These requirements and limits are designed to provide reasonable protection against harmful interference when the product is operated in its intended operational electromagnetic environment.

This product is intended for use in industrial locations. There is no guarantee that harmful interference will not occur in a particular installation, when the product is connected to a test object, or if the product is used in residential areas. To minimize the potential for the product to cause interference to radio and television reception or to experience unacceptable performance degradation, install and use this product in strict accordance with instructions in the product documentation.

Furthermore, any changes or modifications to the product not expressly approved by NI could void your authority to operate it under your local regulatory rules.

Caution To ensure the specified EMC performance, you must install PXI EMC Filler Panels (NI part number 778700-01) in adjacent chassis slots. For more information about installing PXI EMC filler panels in your system, refer to the *Appendix: Installing EMI Controls* section of this document.

Caution To ensure the specified EMC performance, operate this product only with shielded cables and accessories.

Caution To ensure the specified EMC performance, install the included snap-on ferrite bead (NI part number 711856-01) on any cable attached to the AUX I/O connector in accordance with the instructions listed in the *Appendix: Installing EMI Controls* section.

Caution This product is sensitive to electrostatic discharge (ESD). To ensure the specified EMC performance, follow the programming instructions listed at the end of the *Using Your Device with a LabVIEW FPGA Example VI* and *Creating a LabVIEW Project and Running a VI on an FPGA Target* sections of this document.

How to Use Your NI FlexRIO Documentation Set

Refer to Figure 2 and Table 1 for information about how to use your NI FlexRIO documentation set.

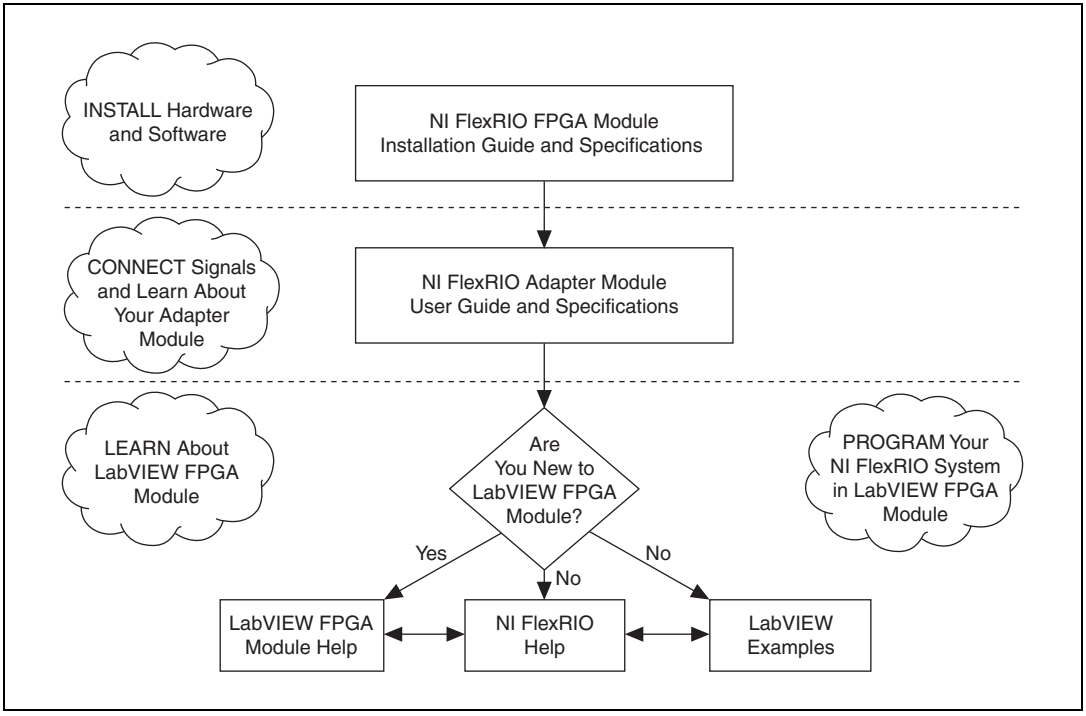


Figure 2. How to Use Your NI FlexRIO Documentation Set

Table 1. NI FlexRIO Documentation Locations and Descriptions

Document	Location	Description
NI FlexRIO FPGA Module Installation Guide and Specifications[*]	Available in your FPGA module hardware kit and from the Start Menu.	Contains installation instructions for your NI FlexRIO system and specifications for your FPGA module.
NI xxxxR User Guide and Specifications[*]	Available from the Start Menu.	Contains signal information, examples, and specifications for your adapter module.
LabVIEW FPGA Module Help[*]	Embedded in *LabVIEW Help*.	Contains information about the basic functionality of LabVIEW FPGA Module.
NI FlexRIO Help[*]	Embedded in *LabVIEW FPGA Module Help*.	Contains FPGA module, adapter module, and CLIP configuration information.
LabVIEW Examples	Available in NI Example Finder.	Contains examples of how to run FPGA VIs and Host VIs on your device.
Other Useful Information on `ni.com`		
`ni.com/ipnet`	Contains LabVIEW FPGA functions and intellectual property to share.	
`ni.com/flexrio`	Contains product information and data sheets for NI FlexRIO devices.	
[*] These documents are also available at `ni.com/manuals`.		

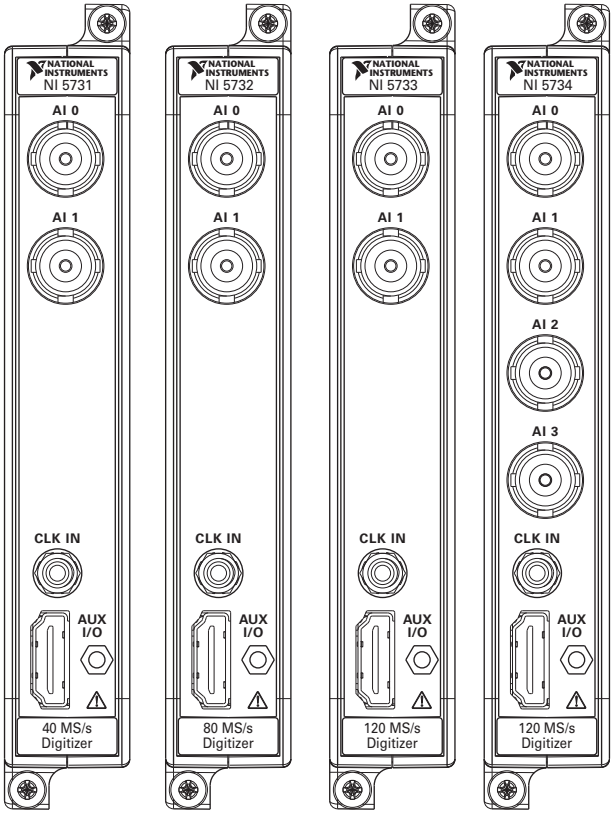
Front Panel and Connector Pinouts

Front Panel

Table 2 shows the front panel connector and signal descriptions for the NI-5731/5732/5733/5734. Refer to the *Specifications* section of this document for additional signal information.

Table 2. NI-5731/5732/5733/5734 Front Panel Connectors

Connector	Signal Description
AI 0	50 Ω single-ended analog input channel 0.
AI 1	50 Ω single-ended analog input channel 1.
AI 2	50 Ω single-ended analog input channel 2 (NI-5734 only).
AI 3	50 Ω single-ended analog input channel 3 (NI-5734 only).
CLK IN	Reference or external clock input, 50 Ω single-ended.
AUX I/O	Refer to Table 3 for the signal list and descriptions.

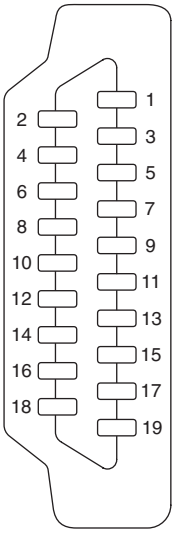


Caution Connections that exceed any of the maximum ratings of any connector on the NI-5731/5732/5733/5734 can damage the device and the chassis. NI is *not* liable for any damage resulting from such signal connections. For the maximum input and output ratings for each signal, refer to the *Specifications* section of this document.

AUX I/O Connector

Table 3 shows the pin assignments for the AUX I/O connector on the NI-5731/5732/5733/5734.

Table 3. NI-5731/5732/5733/5734 AUX I/O Connector Pin Assignments

AUX I/O Connector	Pin	Signal	Signal Description
	1	DIO Port 0 (0)	Bidirectional single-ended digital I/O data channel.
	2	GND	Ground reference for signals.
	3	DIO Port 0 (1)	Bidirectional single-ended digital I/O data channel.
	4	DIO Port 0 (2)	Bidirectional single-ended digital I/O data channel.
	5	GND	Ground reference for signals.
	6	DIO Port 0 (3)	Bidirectional single-ended digital I/O data channel.
	7	DIO Port 1 (0)	Bidirectional single-ended digital I/O data channel.
	8	GND	Ground reference for signals.
	9	DIO Port 1 (1)	Bidirectional single-ended digital I/O data channel.
	10	DIO Port 1 (2)	Bidirectional single-ended digital I/O data channel.
	11	GND	Ground reference for signals.
	12	DIO Port 1 (3)	Bidirectional single-ended digital I/O data channel.
	13	PFI 0	Bidirectional single-ended digital I/O data channel.
	14	NC	No connect.
	15	PFI 1	Bidirectional single-ended digital I/O data channel.
	16	PFI 2	Bidirectional single-ended digital I/O data channel.
	17	GND	Ground reference for signals.
	18	+5V	+5 V power (10 mA maximum).
	19	PFI 3	Bidirectional single-ended digital I/O data channel.

Caution The AUX I/O connector accepts a standard, third-party HDMI cable, but the AUX I/O port is not an HDMI interface. Do *not* connect the AUX I/O port on the NI-5731/5732/5733/5734 into the HDMI port of another device. NI is *not* liable for any damage resulting from such signal connections.

Block Diagram

Figure 3 shows the NI-5731/5732/5733/5734 block diagram and signal flow to and from the NI-5731/5732/5733/5734 component-level intellectual property (CLIP) by way of the adapter module and the corresponding CLIP in LabVIEW FPGA.

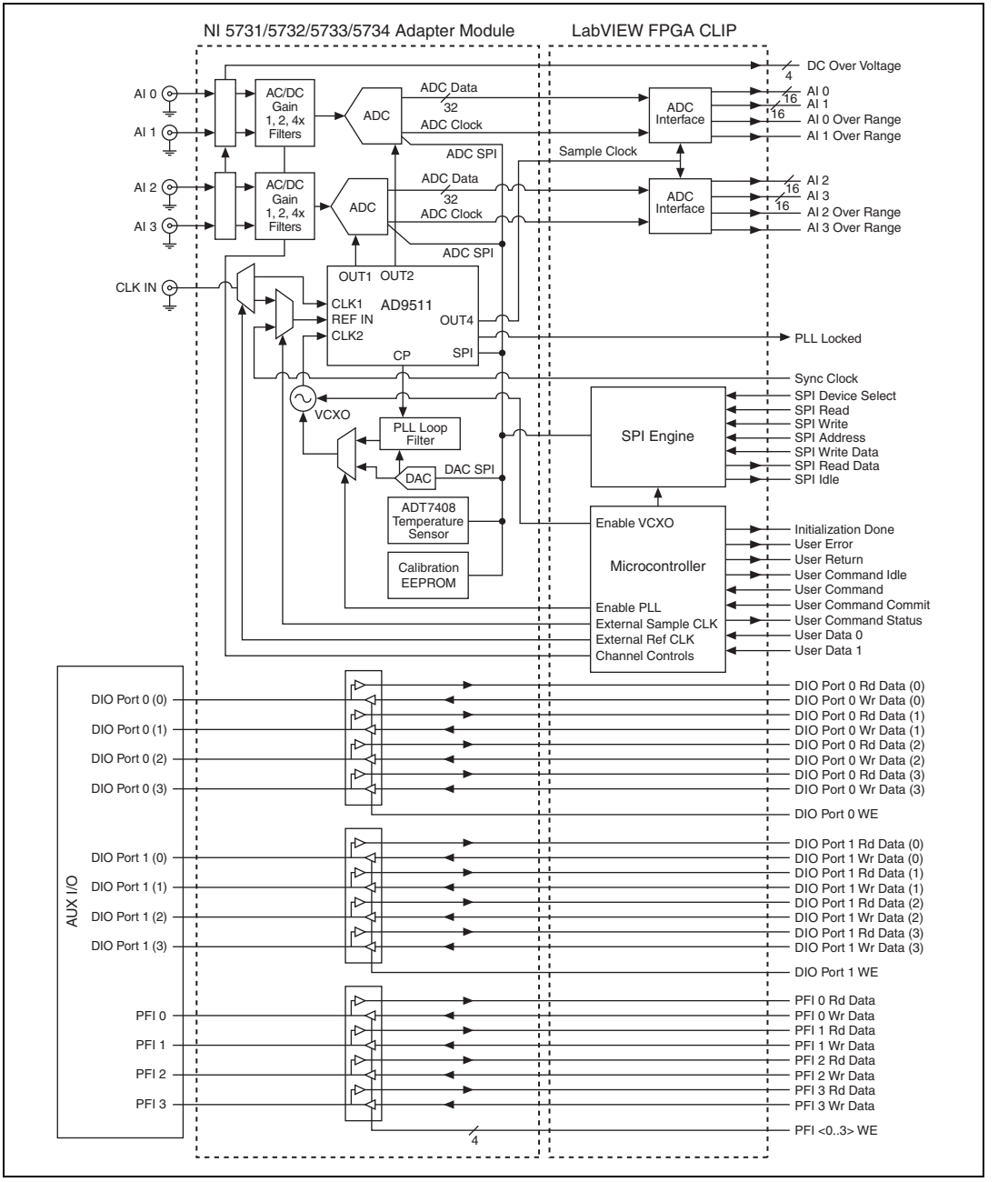


Figure 3. NI-5731/5732/5733/5734 Connector Signals and CLIP Signal Block Diagram

The LabVIEW FPGA Module includes a feature for HDL IP integration called CLIP. NI FlexRIO devices support two types of CLIP: user-defined and socketed.

- *User-defined CLIP* allows users to insert HDL IP into an FPGA target, enabling VHDL code to communicate directly with an FPGA VI.
- *Socketed CLIP* provides the same IP integration functionality of the user-defined CLIP, but also allows the CLIP to communicate directly with circuitry external to the FPGA. Adapter module socketed CLIP allows your IP to communicate directly with both the FPGA VI and the external adapter module connector interface.

Figure 4 shows the relationship between an FPGA VI and CLIP.

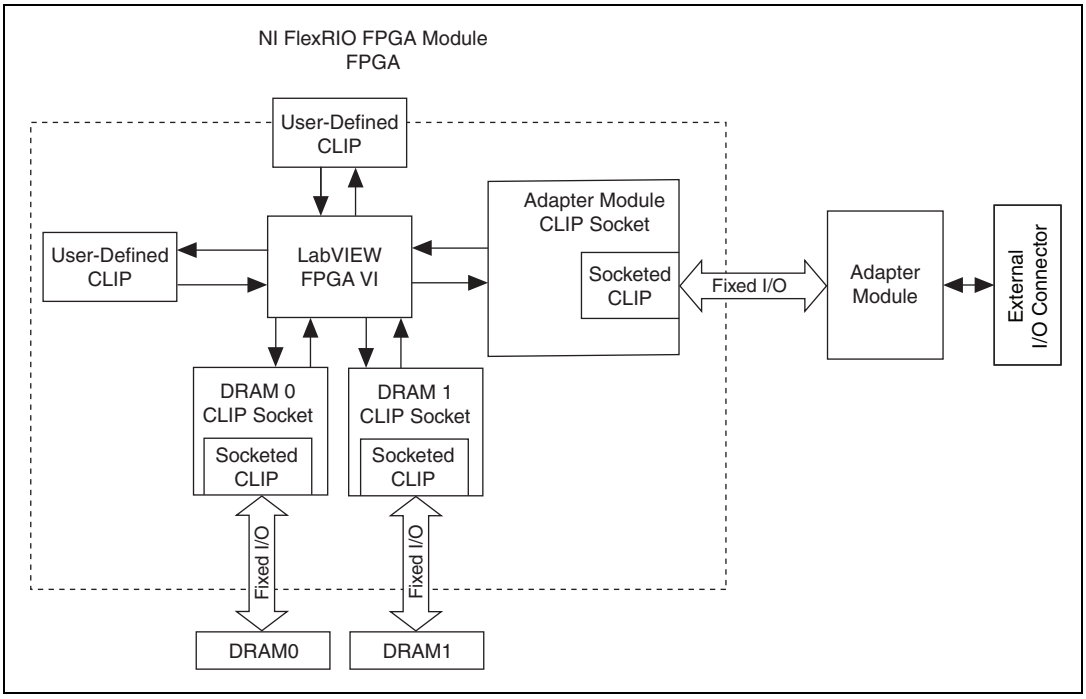


Figure 4. CLIP and FPGA VI Relationship

The NI-5731/5732/5733/5734 ships with socketed CLIP items that are used to add module I/O to the LabVIEW project.

The NI-5731/5732/5733/5734 CLIP items provides access to two analog input channels (four analog input channels on the NI-5734), eight bidirectional DIO channels, four bidirectional PFI channels, and an input clock selector that can be configured to use one of the following settings:

- Internal Sample clock
- Internal Sample clock locked to an external Reference clock through the CLK IN connector
- External Sample clock through the CLK IN connector
- Internal Sample clock locked to an external Reference clock through Sync Clock

The CLIP items also contain an engine to program the ADC and clock, either through predetermined settings for an easier instrument setup or through a raw SPI address and data signals for a more advanced setup. In the LabVIEW FPGA Module, analog input data is accessed using a U16 data type (left justified). The DIO signals are grouped into two ports of four signals each and are accessed using a U8 data type and Boolean write enable signal. The four PFI signals are accessed individually using Booleans.

Refer to the *NI FlexRIO Help* for more information about NI FlexRIO CLIP items, configuring the NI-5731/5732/5733/5734 with a socketed CLIP, and a list of available socketed CLIP signals.

Cables

- Use any shielded 50 Ω coaxial cable of less than 3 meters in length with a BNC plug end to connect to the AI 0, AI 1, AI 2, and AI 3 connectors on the NI-5731/5732/5733/5734 front panel.
- Use any shielded 50 Ω coaxial cable of less than 3 meters in length with an SMB plug end to connect to the CLK IN connector.
- Use any HDMI cable with the provided ferrite bead to connect to the digital I/O and PFI signals on the AUX I/O connector.

Caution To ensure the specified EMC performance, install the included snap-on ferrite bead (NI part number 711856-01) on any cable attached to the AUX I/O connector in accordance with the instructions listed in the *Appendix: Installing EMI Controls* section.

Clocking

The NI-5731/5732/5733/5734 clocks control the sample rate and other timing functions on the device. Table 4 contains information about the possible NI-5731/5732/5733/5734 clock resources.

Table 4. NI-5731/5732/5733/5734 Clock Sources

Clock Configuration	Supported Sample Rates	External Clock Type	External Clock Frequency	Description
Internal Clock PLL Off	NI-5731 = 40 MS/s NI-5732 = 80 MS/s NI-5733 = 120 MS/s NI-5734 = 120 MS/s	—	—	The internal VCXO acts as a free-running clock.
Internal Clock PLL On (IoModSyncClk)	NI-5731 = 40 MS/s NI-5732 = 80 MS/s NI-5733 = 120 MS/s NI-5734 = 120 MS/s	—	10 MHz	The internal VCXO locks to IoModSyncClk (Sync Clock), which is provided only through the backplane of supported devices.
Internal Clock PLL On (CLK IN)	NI-5731 = 40 MS/s NI-5732 = 80 MS/s NI-5733 = 120 MS/s NI-5734 = 120 MS/s	Reference clock	10 MHz	The internal VCXO locks to an external Reference clock, which is provided through the CLK IN front panel connector.

Table 4. NI-5731/5732/5733/5734 Clock Sources (Continued)

Clock Configuration	Supported Sample Rates	External Clock Type	External Clock Frequency	Description
External Clock (CLK IN)	The supported sample rate is equal to the external clock frequency.	Sample clock	NI-5731 Min = 3 MHz NI-5731 Max = 40 MHz NI-5732 Min = 20 MHz* NI-5732 Min = 10 MHz† NI-5732 Max = 80 MHz NI-5733 Min = 50 MHz NI-5733 Max = 120 MHz NI-5734 Min = 50 MHz NI-5734 Max = 120 MHz	An external Sample clock can be provided through the CLK IN front panel connector.

* Duty Cycle Stabilizer (DCS) enabled. DCS enabled is the default setting for all NI-5731/5732/5733/5734 CLIP items. You can disable the DCS by adjusting register 9 in the ADC.

† DCS disabled.

Note Specifications for the NI-5731/5732/5733/5734 adapter modules were characterized only at the maximum sample rates.

Note For more information about configuring clocks, refer to the respective CLIP Help section for your device in the *NI FlexRIO Help*.

Using Your Device with a LabVIEW FPGA Example VI

Note You must install the NI FlexRIO Adapter Module Support software before running this example. Refer to the *NI FlexRIO FPGA Module Installation Guide and Specifications* for more information about installing your software.

The NI FlexRIO Adapter Module Support software includes a variety of example projects to help get you started creating your LabVIEW FPGA application. This section explains how to use an existing LabVIEW FPGA example project to generate and acquire samples with the NI-5731/5732/5733/5734R. This example requires at least one BNC cable for connecting signals to your device.

Note The examples available for your device are dependent on the version of the software and driver you are using. For more information about which software versions are compatible with your device, visit `ni.com/info` and enter `rdsoftwareversion` as the Info Code.

Each NI-5731/5732/5733/5734R example project includes the following components:

- A LabVIEW FPGA VI that can be compiled and run on the FPGA embedded in the hardware
- A VI that runs on Windows that interacts with the LabVIEW FPGA VI

Note In the LabVIEW FPGA Module software, NI FlexRIO adapter modules are referred to as *IO Modules*.

Complete the following steps to run an example that acquires a waveform on AI 0 of the NI-5731/5732/5733/5734.

1. Connect one end of an BNC cable to AI 0 on the front panel of the NI-5731/5732/5733/5734 and the other end of the cable to your device under test (DUT).
2. Launch LabVIEW.
3. In the **Getting Started** window, click **Find Examples** to display the NI Example Finder.
4. In the **NI Example Finder** window, select **Hardware Input and Output»FlexRIO»IO Modules» NI-573X»NI-573*y*** (where *y* represents the device number you are using).
5. Select **NI-573*y* - Getting Started.lvproj**. Wait for the project to finish opening.
6. In the **Project Explorer** window, open **NI-573*y* - Getting Started (Host).vi** under **My Computer**. The host VI opens. The Open FPGA VI Reference function in this VI uses the NI-7952R as the FPGA target by default. If you are using an NI FlexRIO FPGA module other than the NI-7952R, complete the following steps to change to the FPGA VI to support your target.
   a. Select **Window»Show Block Diagram** to open the VI block diagram.
   b. On the block diagram, right-click the **Open FPGA VI Reference** (PXI-7952R) function and select **Configure Open FPGA VI Reference**.
   c. In the **Configure Open FPGA VI Reference** dialog box, click the **Browse** button next to the **Bitfile** button.
   d. In the **Select Bitfile** dialog box that opens, select the bitfile for your desired target. The bitfile name is based on the adapter module, example type, and FPGA module.
   e. Click the **Select** button.
   f. Click **OK** in the **Configure Open FPGA VI Reference** dialog box.
   g. Save the VI.
7. On the front panel, in the **RIO Resource** pull-down menu, select a resource that corresponds with the target configured in step 6.
8. Select **AI 0** in the **AI Channel** control.
9. Set the **Trigger Level (V)** and the **Record Size** controls to the desired value.
10. In the **Trigger Type** control, you can select either **Software Trigger** or **Data Edge**. If you select **Software Trigger**, the VI acquires data every time you click the **Software Trigger** button on the front panel of the VI. If you select **Data Edge**, the VI acquires data every time an edge occurs.
11. Set the **Sample Rate** control to the default sample rate of your device.

Note The **Sample Rate** control does not change the sample rate of your device; it only adjusts the time display.

12. Click the **Run** button to run the VI.
13. Click the **Software Trigger** button if you selected **Software Trigger** in the **Trigger Type** control. The VI acquires data and displays the captured waveform on the **Acquired Waveform** graph as shown in Figure 5.
14. Click the **STOP** button to stop the VI. Close the VI.

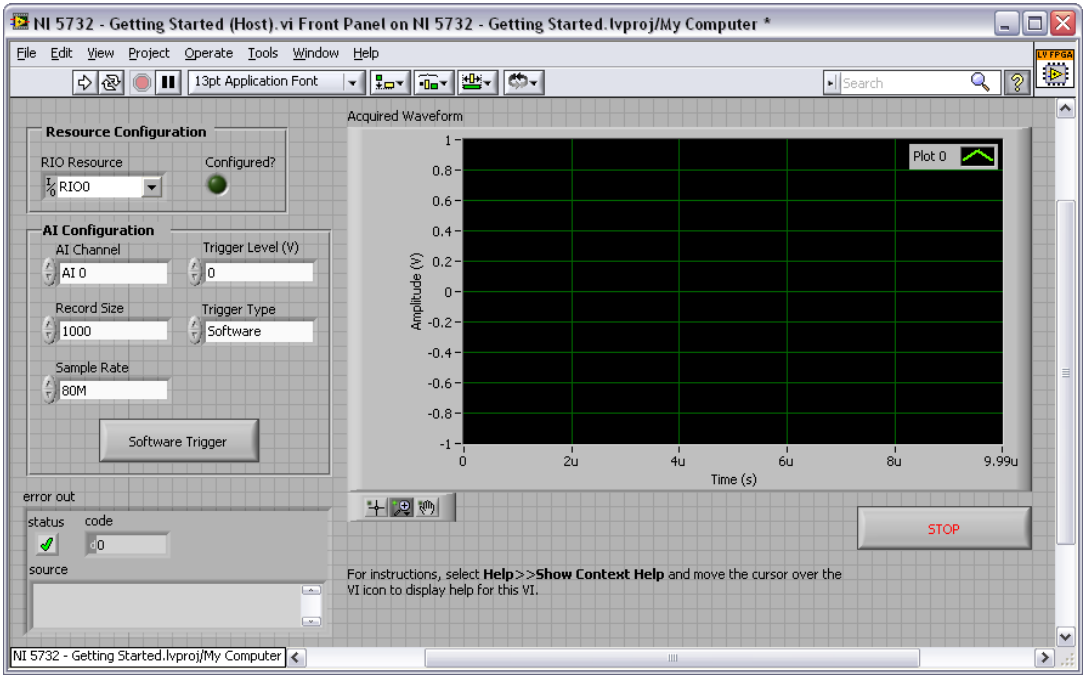


Figure 5. NI-573*x* - Getting Started (Host) VI Front Panel

Note **(NI-5731 Only)** ESD events can affect the NI-5731 Sample clock, which can cause error `-50400` when performing DMA transfers or result in other clock performance and timeout errors when acquiring data on the NI-5731. To ensure that the NI-5731 self-recovers from this error, the host and FPGA VIs must be able to trap these timeout errors and reinitialize the FPGA. The following two steps describe how to self-recover the NI-5731:

1. For more information about how to trap the error, visit the KnowledgeBase at `ni.com/kb`, enter `3BPD5HRY`, and select the article, *Ignoring a Particular Error in an Error Cluster in LabVIEW.*
2. To reinitialize the FPGA, refer to the *Reset (Invoke Method)* topic in the *NI FPGA Module Help* file, available in LabVIEW and at `ni.com/manuals`.

Creating a LabVIEW Project and Running a VI on an FPGA Target

This section explains how to set up your target and create an FPGA VI and host VI for data communication. For more detailed information about acquiring data on your NI-5731/5732/5733/5734, refer to the device specific examples available in NI Example Finder.

Creating a Project

1. Launch LabVIEW, or if LabVIEW is already running, select **File»New**.
2. In the **New** dialog box, select **Project»Empty Project** and click **OK**. The new project opens in the **Project Explorer** window.
3. Save the project as `573xSampleAcq.lvproj`.

Creating an FPGA Target VI

1. In the **Project Explorer** window, right-click **My Computer** and select **New»Targets and Devices**.
2. In the **Add Targets and Devices on My Computer** dialog box, select the **Existing Target or Device** button and expand **FPGA Target**. The target is displayed.
3. Select your device and click **OK**. The target and target properties are loaded into the **Project Explorer** window.
4. In the **Project Explorer** window, expand **FPGA Target (RIO*x*, PXI-79*xx*R)**.
5. Right-click **FPGA Target (RIO*x*, PXI-79*xx*R)** and select **New»FPGA Base Clock**.
6. In the **Resource** pull-down menu, select **IO Module Clock 0**.
7. Enter the default Sample clock rate for your device (`40`, `80`, or `120`) in the **Compile for single frequency** control and click **OK**.
8. Right-click **IO Module** in the **Project Explorer** window and select **Properties**.
9. Select the NI-573*x* from the IO Module list. The available CLIP for the NI-5731/5732/5733/5734 is displayed in the **General** category of the Component Level IP pane. If the information in the **General** category is dimmed, select the **Enable IO Module** checkbox.
10. Select **NI-573x CLIP** in the **Name** list box of the Component Level IP section.
11. In the **Clock Selections** category, leave **Clk40** configured as the **Top-Level Clock**. This step is necessary to compile the FPGA VI correctly.
12. Click **OK**.

Note Configuring this clock is required for proper CLIP operation. Refer to the NI-5731/5732/5733/5734 CLIP topics in the *NI FlexRIO Help* for more information about configuring your clocks.

13. In the **Project Explorer** window, right-click the FPGA target and select **New»VI**. A blank VI opens.
14. Select **Window»Show Block Diagram** to open the VI block diagram.
15. In the **Project Explorer** window, expand the **IO Module (NI-573x: NI-573x)** tree view.
16. Drag **AI 0** to the block diagram.
17. Add a Timed Loop structure around the single node.
18. Wire an indicator to the output terminal of the **IO Module\AI 0 Data N** node.
19. Wire an **FPGA Clock Constant** to the input node of the Timed Loop. Set this constant to **IO Module Clock 0**.

Your block diagram should now resemble the block diagram in Figure 6.

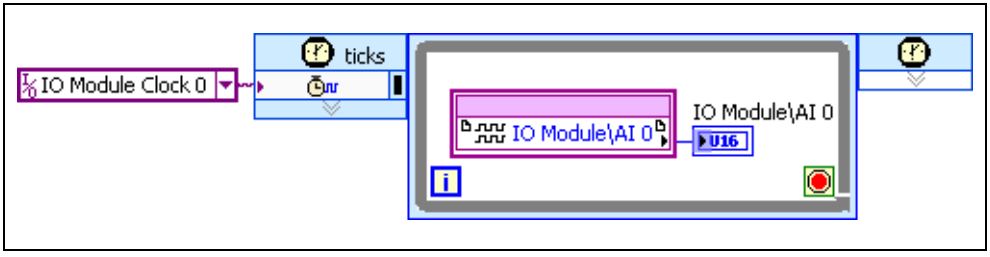


Figure 6. 5731/5732/5733/5734SampleAcq (FPGA).vi Block Diagram

Tip Click the **Clean Up Diagram** button on the toolbar to cleanly organize the VI block diagrams.

20. Save the VI as `573xSampleAcq (FPGA).vi`.
21. Click the **Run** button. LabVIEW creates a default build specification and begins compiling the VI. The **Generating Intermediate Files** window opens and displays the code generation progress. Next, the **Compilation Status** window opens and displays the progress of the compilation. The compilation takes several minutes.
22. Click **Close** in the **Compilation Status** window.
23. Save and close the VI.
24. Save the project.

Creating a Host VI

1. In the **Project Explorer** window, right-click **My Computer** and select **New»VI**. A blank VI opens.
2. Select **Window»Show Block Diagram** to open the VI block diagram.
3. Place the Open FPGA VI Reference function, located on the **FPGA Interface** palette, on the block diagram.
4. Right-click the Open FPGA VI Reference function and select **Configure Open FPGA VI Reference**.
5. In the **Configure Open FPGA VI Reference** dialog box, select VI in the **Open** section.
6. In the **Select VI** dialog box that opens, select **573xSampleAcq (FPGA).vi** under your device and click **OK**.
7. Click **OK** in the **Configure Open FPGA VI Reference** dialog box. The target name appears under the Open FPGA VI Reference function in the block diagram.
8. Add a While Loop to the block diagram. Place it to the right of the Open FPGA VI Reference function.
9. Right-click the conditional terminal inside the While Loop and select **Create Control** to create a STOP button on the VI front panel window.
10. Add the Read/Write Control function, located on the **FPGA Interface** palette, inside the While Loop.
11. Wire the **FPGA VI Reference Out** output terminal of the Open FPGA VI Reference function to the **FPGA VI Reference In** input terminal on the Read/Write Control function.
12. Wire the **error out** terminal of the Open FPGA VI Reference function to the **error in** control of the Read/Write Control function.
13. Configure the Read/Write Control function by clicking the terminal section labeled **Unselected**, and selecting **IO Module/AI 0 Data N**.
14. Wire an indicator to the output terminal of the IO Module\AI 0 Data N node.
15. Add the Close FPGA VI Reference function, located on the **FPGA Interface** palette, to the right of the While Loop on the block diagram.
16. Wire the **FPGA VI Reference Out** terminal of the Read/Write Control function to the **FPGA VI Reference In** terminal of the Close FPGA VI Reference function.
17. Wire the **error out** terminal of the Read/Write Control function to the **error in** terminal of the Close FPGA VI Reference function.

Your block diagram should now resemble the block diagram in Figure 7.

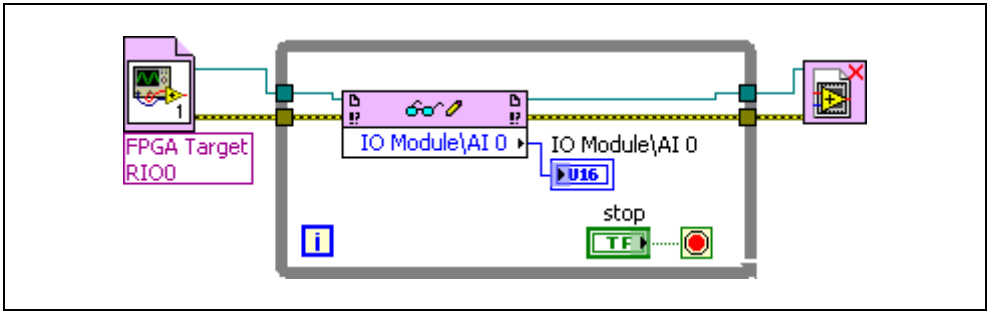


Figure 7. 573xSampleAcq(Host).vi Block Diagram

18. Save the VI as `573xSampleAcq(Host).vi`.

Running the Host VI

1. Connect one end of an BNC cable to AI 0 on the front panel of the NI-5731/5732/5733/5734 and the other end of the cable to your DUT.
2. Open the front panel of `573xSampleAcq(Host).vi`.
3. Click the **Run** button to run the VI.
4. The VI acquires data from the DUT on AI 0 Data N.
5. Click the **STOP** button on the front panel and close the VI.

Note **(NI-5731 Only)** ESD events can affect the NI-5731 Sample clock, which can cause error `-50400` when performing DMA transfers or result in other clock performance and timeout errors when acquiring data on the NI-5731. To ensure that the NI-5731 self-recovers from this error, the host and FPGA VIs must be able to trap these timeout errors and reinitialize the FPGA. The following two steps describe how to self-recover the NI-5731:

1. For more information about how to trap the error, visit the KnowledgeBase at `ni.com/kb`, enter `3BPD5HRY`, and select the article, *Ignoring a Particular Error in an Error Cluster in LabVIEW.*
2. To reinitialize the FPGA, refer to the *Reset (Invoke Method)* topic in the *NI FPGA Module Help* file, available in LabVIEW and at `ni.com/manuals`.

Specifications

This section lists the specifications of the NI FlexRIO adapter module (NI-5731/5732/5733/5734). Pair these specifications with the specifications listed in the *NI FlexRIO FPGA Module Installation Guide and Specifications*. For more information about safety and electromagnetic compatibility refer to the *Read Me First: Safety and Electromagnetic Compatibility* document included in your hardware kit or available at `ni.com/manuals`.

Note All numeric specifications are typical unless otherwise noted. All graphs illustrate the performance of a representative module.

Typical values describe useful product performance that are not covered by warranty. Typical values cover the expected performance of units over ambient temperature ranges of 23 ±5 °C with an 85% confidence level, based on measurements taken during development or production.

Note Specifications for the NI-5731/5732/5733/5734 adapter modules were characterized only at the maximum sample rates.

Analog Input (AI 0, AI 1, AI 2, and AI 3)

General Characteristics

Number of channels ..... Two (four channels on the NI-5734)

Connector type ..... BNC

Input type ..... Simultaneously sampled, singled-ended

Input impedance ..... 50 Ω, per connector

Input coupling (software selectable) ..... AC or DC

Gain (software selectable) ..... 0 dB, 6 dB, or 12 dB

Signal paths (software selectable) ..... Filter bypass, 7th-order Elliptic filter, 7th-order Bessel filter

Digital data resolution (16-bit, left-justified, unsigned, binary data)

- NI-5731 ..... 12 bit
- NI-5732 ..... 14 bit
- NI-5733/5734 ..... 16 bit

ADC part number[1]

- NI-5731 ..... AD9231BCPZ-40
- NI-5732 ..... AD9258BCPZ-80
- NI-5733/5734 ..... AD9268BCPZ-125

Absolute maximum voltage ..... ±10 V DC, 10 V_{pk-pk} AC

DC overvoltage disconnect ..... ±2 V DC (exceeding this voltage forces AC-mode)

Typical Specifications

ADC DC offset

- NI-5731 ..... ±5.2 mV
- NI-5732 ..... ±6.6 mV
- NI-5733/5734 ..... ±7.1 mV

DC-coupled common-mode output ..... ±0.8 mV (50 Ω terminated)

Full Scale Input

Table 5. Full Scale Input

Device	Gain = 0 dB	Gain = 6 dB (FS at 0 dB divided by 2)	Gain = 12 dB (FS at 0 dB divided by 4)
NI-5731	2.070 V_{pk-pk}	1.035 V_{pk-pk}	0.5175 V_{pk-pk}
NI-5732	2.055 V_{pk-pk}	1.028 V_{pk-pk}	0.5138 V_{pk-pk}
NI-5733/5734	2.085 V_{pk-pk}	1.043 V_{pk-pk}	0.5212 V_{pk-pk}

[1] For additional information about the ADC within your device, use the listed part number to locate the appropriate Analog Devices data sheet at www.analog.com.

DC Gain Error

Table 6. DC Gain Error (Full Scale)

Device	Gain = 0 dB	Gain = 6 dB	Gain = 12 dB
NI-5731	±0.9%	±1.2%	±1.7%
NI-5732	±0.5%	±0.8%	±1.4%
NI-5733/5734	±0.6%	±0.8%	±1.5%

Noise

Table 7. Average Noise Density

Device	Gain (dB)	Full Scale (V_{pk-pk})	Average Noise Density		
			(nV/√Hz)	(dBm/Hz)	(dBFS/Hz)
NI-5731	0	2.070	61.5	–131.2	–141.2
	6	1.035	33.0	–136.6	–140.6
	12	0.5175	18.6	–141.6	–139.6
NI-5732	0	2.055	33.4	–136.5	–148.4
	6	1.0275	18.3	–141.7	–147.6
	12	0.51375	10.7	–146.4	–146.3
NI-5733/5734	0	2.085	26.9	–138.4	–148.4
	6	1.0425	14.8	–143.6	–147.6
	12	0.52125	8.6	–148.3	–146.3

Passband

AC-coupling low cut-off frequency (–3 dB).....20 kHz

DC-coupling low cut-off frequency.....0 Hz

Table 8. Passband High Cut-off Frequency (–3 dB)

Device	Filter Bypass	Elliptic Filter	Bessel Filter
NI-5731	120 MHz	15.8 MHz	8.1 MHz
NI-5732	110 MHz	29.6 MHz	16.1 MHz
NI-5733/5734	117 MHz	37.1 MHz	24.1 MHz

Group Delay Flatness

Table 9. Maximum Frequency to 2 ns

Device	Elliptic Filter	Bessel Filter
NI-5731	9 MHz	18 MHz
NI-5732	20 MHz	37 MHz
NI-5733/5734	30 MHz	53 MHz

Signal to Noise Ratio (SNR) [1]

Table 10. SNR [1]

Device	Input	Gain = 0 dB	Gain = 6 dB	Gain = 12 dB
NI-5731	4.9 MHz	67.2 dB	66.6 dB	65.6 dB
NI-5732	9.7 MHz	69.5 dB	68.7 dB	67.4 dB
NI-5733/5734	9.7 MHz	69.6 dB	68.8 dB	67.5 dB

Total Harmonic Distortion (THD) [1]

Table 11. THD [1]

Device	Input	Gain = 0 dB	Gain = 6 dB	Gain = 12 dB
NI-5731	4.6 MHz	–87.1 dBc	–87.1 dBc	–84.1 dBc
NI-5732	9.7 MHz	–83.9 dBc	–87.7 dBc	–89.5 dBc
NI-5733/5734	9.7 MHz	–80.5 dBc	–85.0 dBc	–86.0 dBc

Spurious-Free Dynamic Range (SFDR) [2]

Table 12. SFDR [1]

Device	Input	Gain = 0 dB	Gain = 6 dB	Gain = 12 dB
NI-5731	4.9 MHz	–87 dBc	–87 dBc	–90 dBc
NI-5732	9.7 MHz	–85 dBc	–89 dBc	–91 dBc
NI-5733/5734	9.7 MHz	–83 dBc	–86 dBc	–87 dBc

AI Channel-to-Channel Crosstalk

Note The following crosstalk tables are measured at 0 dB gain with a –1 dBFS 10 MHz signal on the aggressor channel while the other channels are terminated at 50 Ω. When measuring crosstalk at 6 dB and 12 dB gain, the crosstalk is 6 dB and 12 dB worse, respectively.

[1] Measured at –1 dBFS.

[2] Measured at –1 dBFS.

Table 13. NI-5731/5732/5733/5734: AI Channel Crosstalk

Aggressor Channel *N* (0..3)	Receiver Channel (50 Ω terminated)					
	Adjacent Channel Path (*N* – 1)			Adjacent Channel Path (*N* + 1)		
	Bypass	Elliptic	Bessel	Bypass	Elliptic	Bessel
Filter Bypass	–102 dB	–97 dB	–100 dB	–98 dB	–89 dB	–81 dB
Elliptic Filter	–102 dB	–77 dB	–81 dB	–104 dB	–79 dB	–77 dB
Bessel Filter	–87 dB	–73 dB	–77 dB	–103 dB	–83 dB	–80 dB

Note For NI-5731/5732 devices only, the crosstalk is 4 dB worse than the values in Table 13 when you configure both channels to use filters.

Table 14. NI-5734 only: AI Channel Crosstalk

Aggressor Channel *N* (0..3)	Receiver Channel (50 Ω terminated)			
	Channel Path (*N* ± 2)		Channel Path (*N* ± 3)	
	Bypass	Elliptic or Bessel Filter	Bypass	Elliptic or Bessel Filter
Filter Bypass	–112 dB	–102 dB	–112 dB	–107 dB
Elliptic Filter	–112 dB	–85 dB	–112 dB	–90 dB
Bessel Filter	–112 dB	–86 dB	–112 dB	–90 dB

Phase adjust DAC range

NI-5731 ..... 406 ± 13 degrees
NI-5732 ..... 427 ± 13 degrees
NI-5733 ..... 429 ± 9 degrees
NI-5734 ..... 429 ± 13 degrees

Frequency adjust DAC range ..... ±100 ppm

Data rate (IOModuleClock0) ..... Sample rate

Measurements

Frequency Response

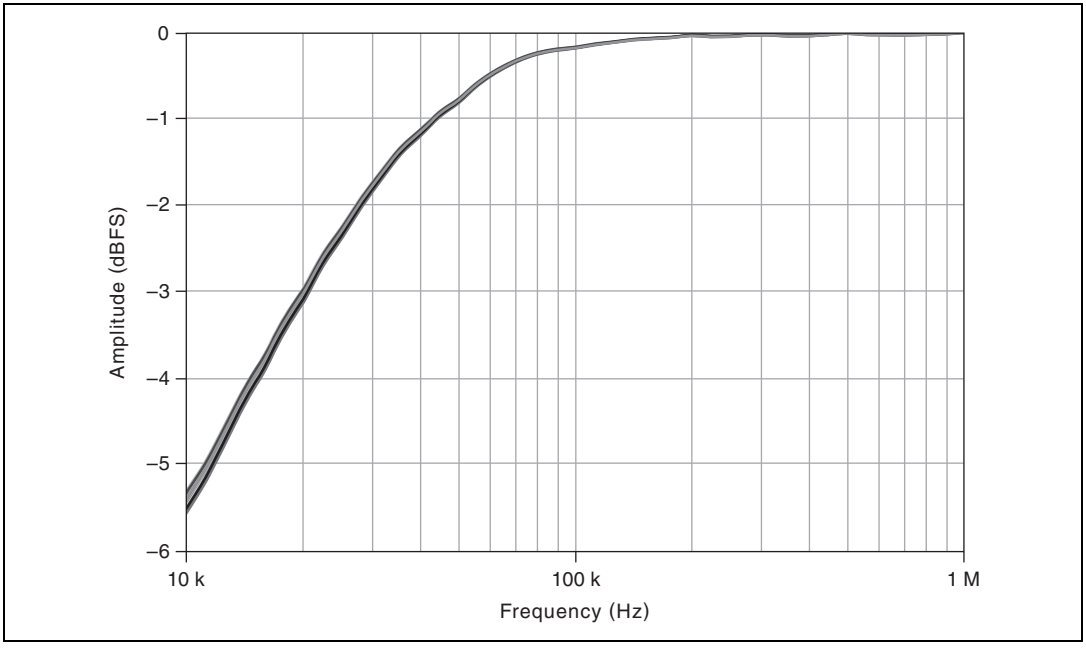


Figure 8. AC-Coupled Low Frequency Response (Multiple Channels Overlaid)

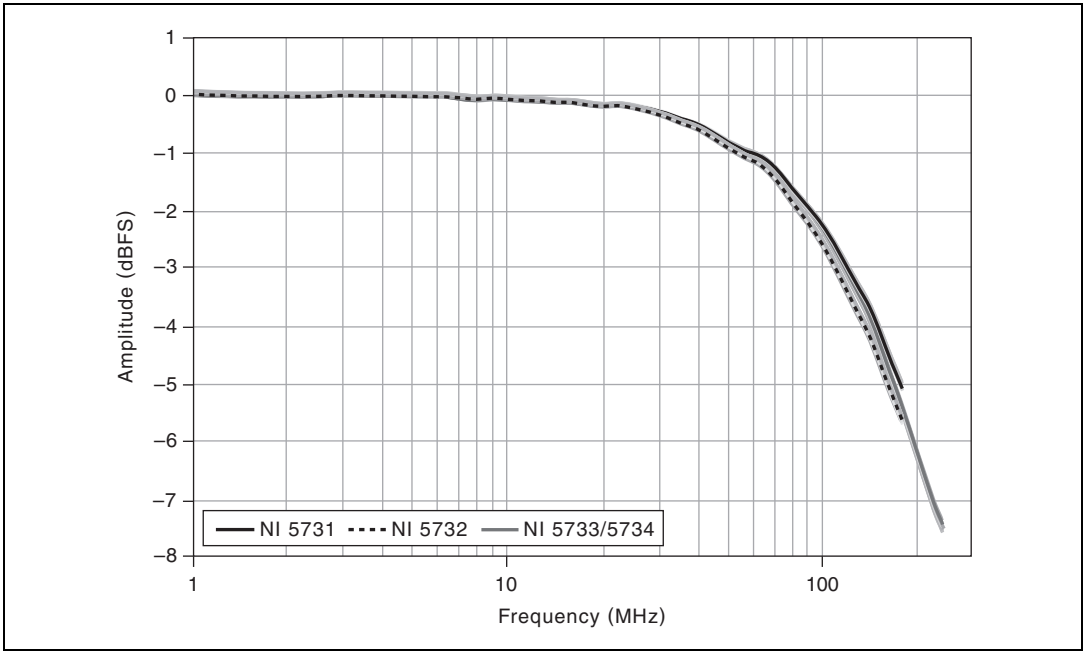


Figure 9. Filter Bypass Frequency Response (Multiple Channels Overlaid)

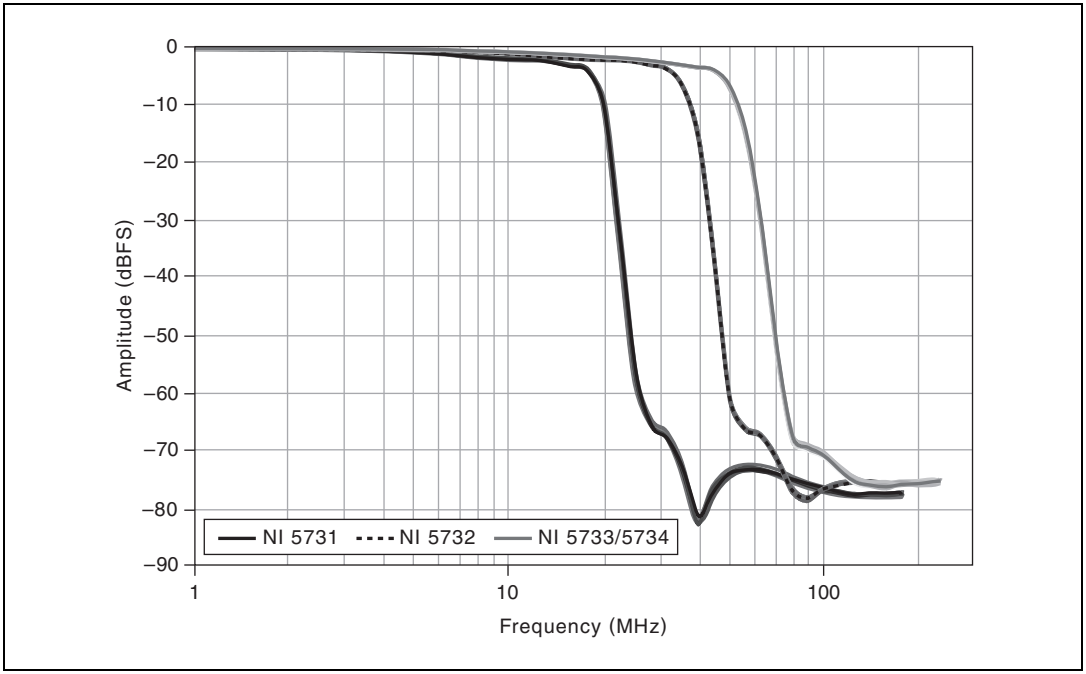


Figure 10. Elliptic Filter Frequency Response (Multiple Channels Overlaid)

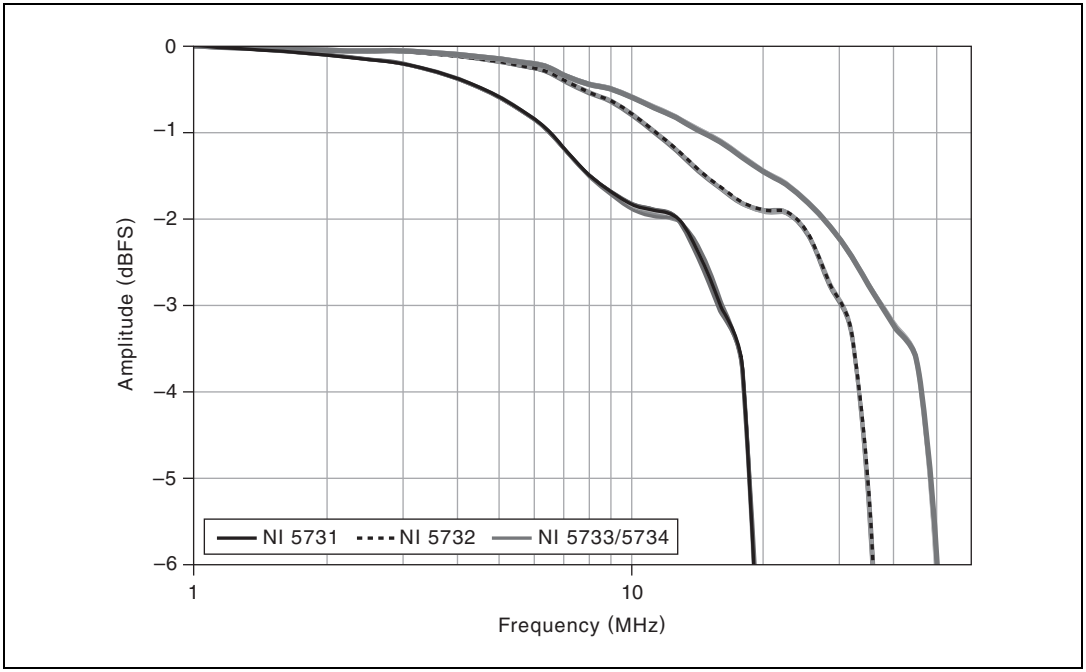


Figure 11. Elliptic Filter Frequency Response: 0 to –6 dB (Multiple Channels Overlaid)

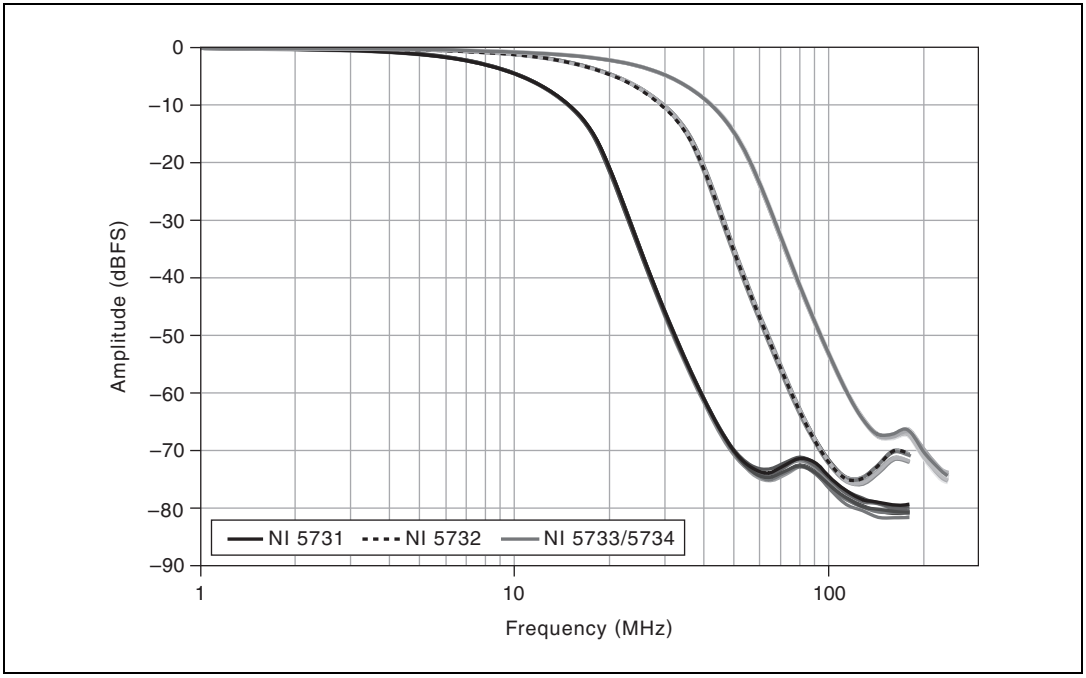


Figure 12. Bessel Filter Frequency Response (Multiple Channels Overlaid)

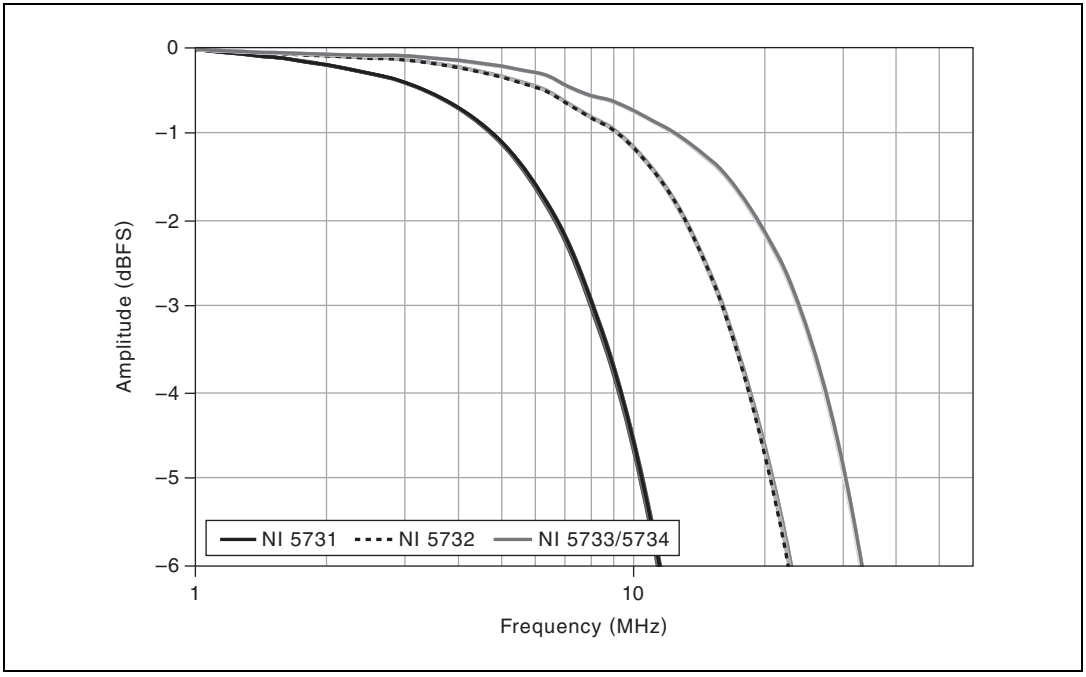


Figure 13. Bessel Filter Frequency Response: 0 to –6 dB (Multiple Channels Overlaid)

NI-5731 Group Delay

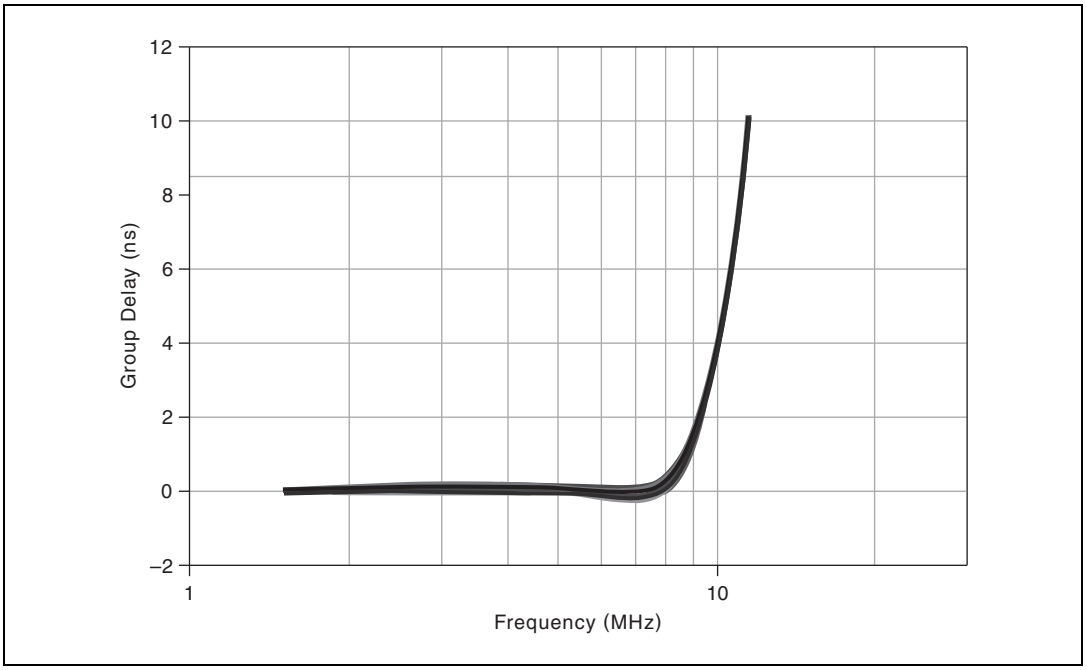


Figure 14. NI-5731 Elliptic Filter Group Delay (12 Channels Overlaid)

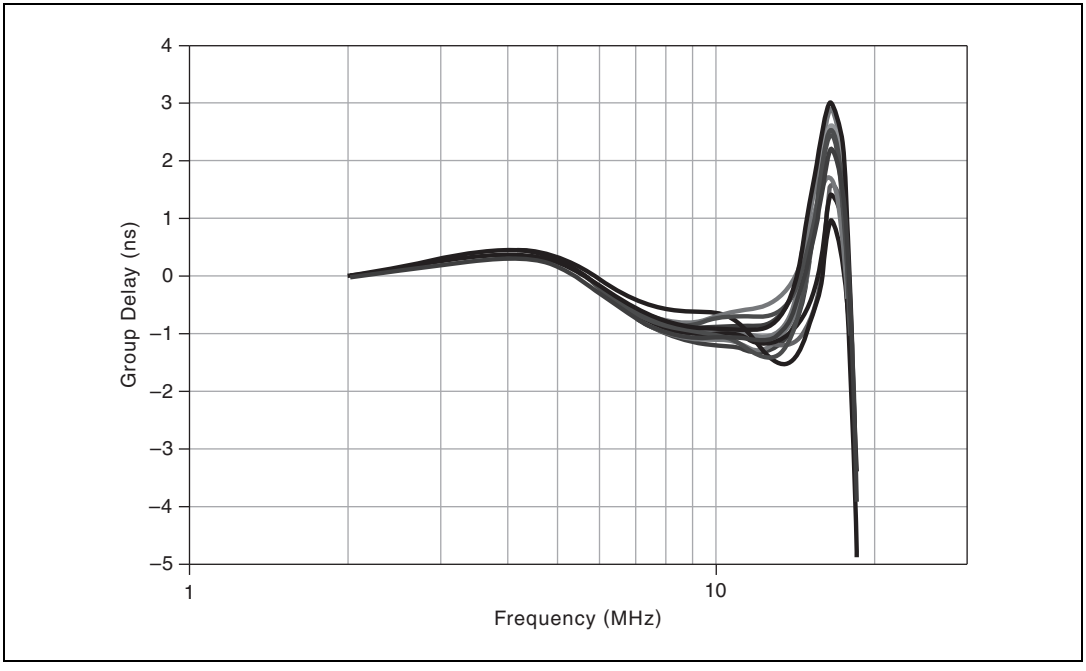


Figure 15. NI-5731 Bessel Filter Group Delay (12 Channels Overlaid)

NI-5732 Group Delay

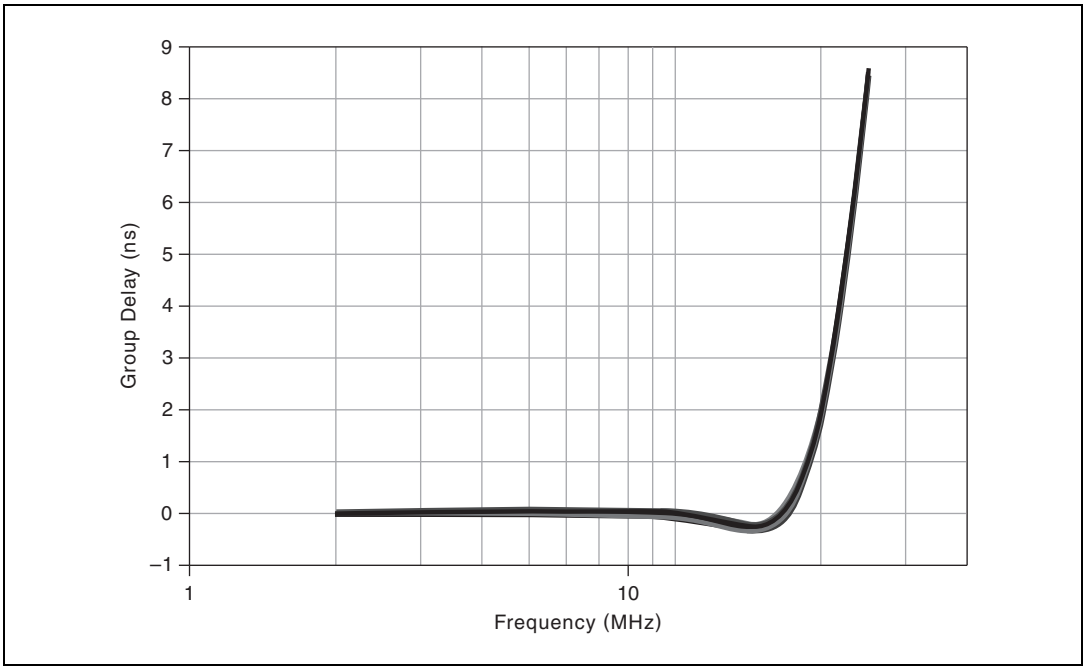


Figure 16. NI-5732 Elliptic Filter Group Delay (12 Channels Overlaid)

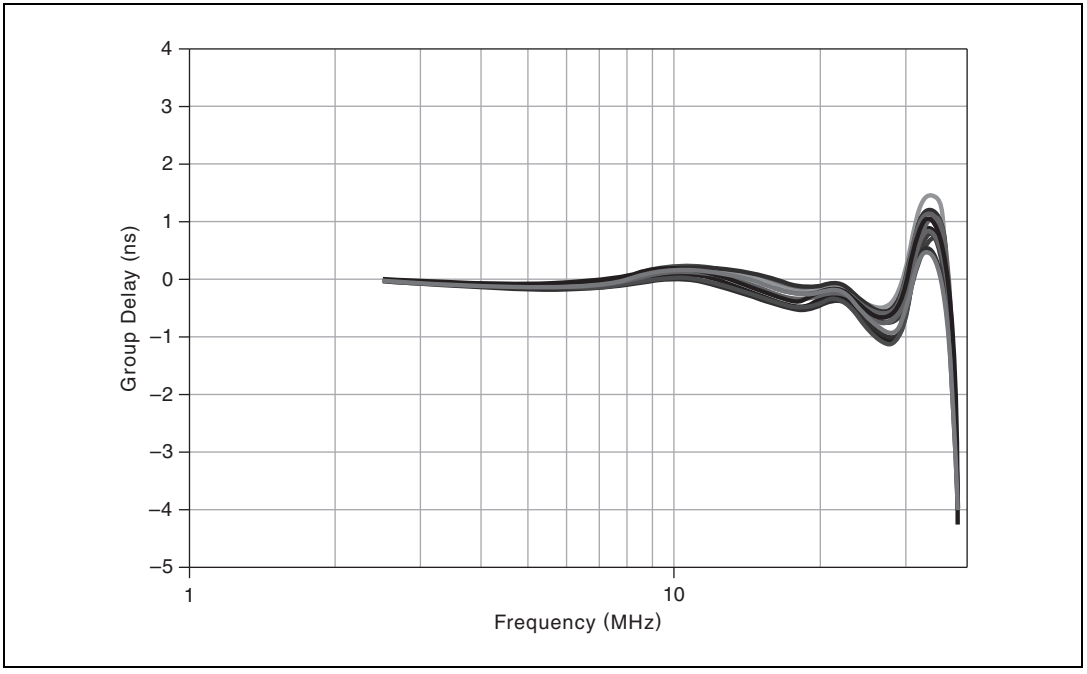


Figure 17. NI-5732 Bessel Filter Group Delay (12 Channels Overlaid)

NI-5733/5734 Group Delay

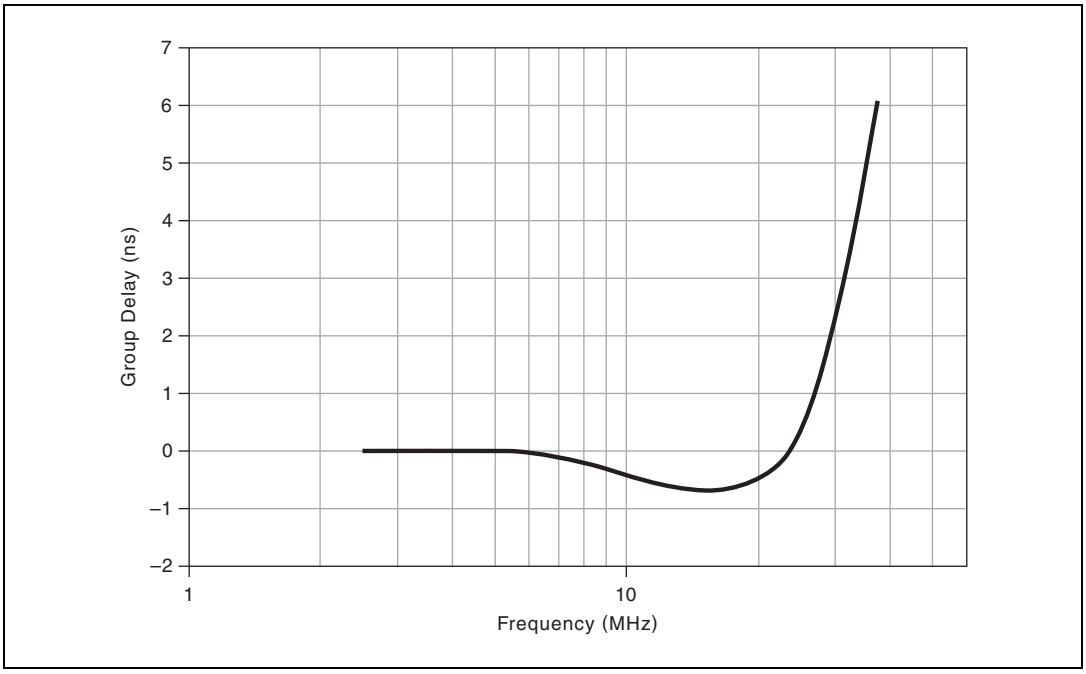


Figure 18. NI-5733/5734 Elliptic Filter Group Delay (44 Channels Overlaid)

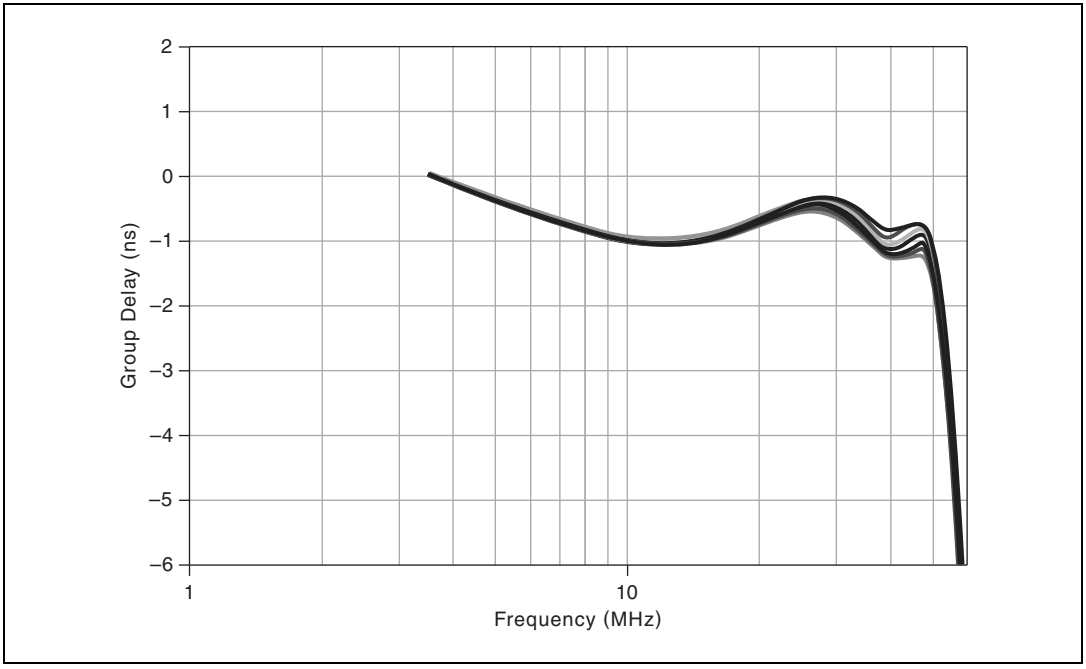


Figure 19. NI-5733/5734 Bessel Filter Group Delay (44 Channels Overlaid)

Analog Input Total Phase Noise

NI-5731

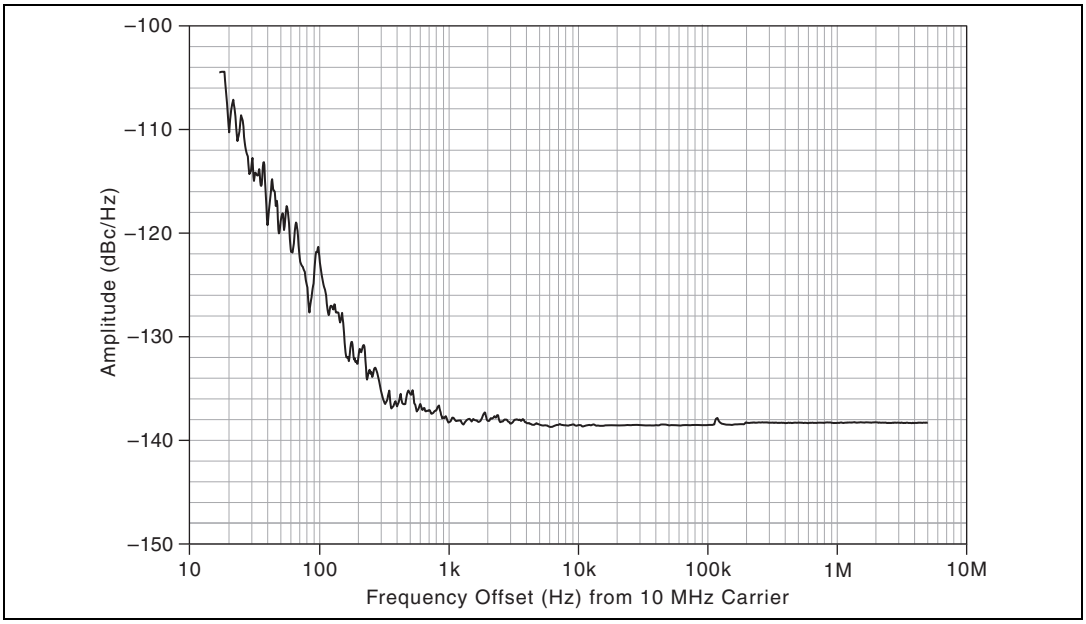


Figure 20. NI-5731 AI Phase Noise (10 MHz Input, PLL Unlocked, Onboard Oscillator, 618 FS RMS Jitter)

NI-5732

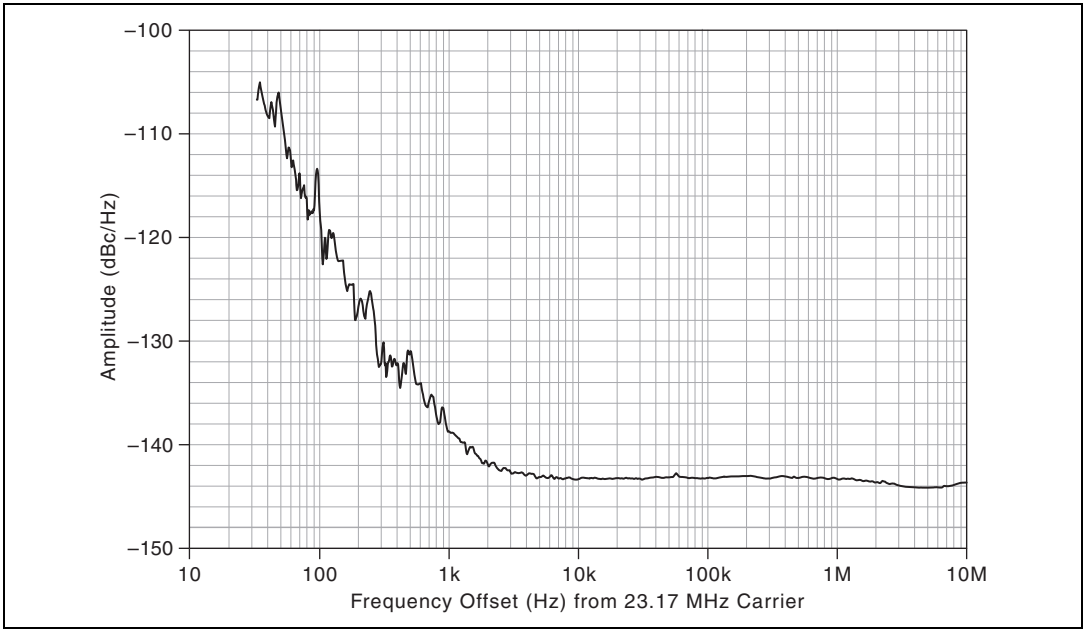


Figure 21. NI-5732 AI Phase Noise (23.17 MHz Input, PLL Unlocked, Onboard Oscillator, 466 FS RMS Jitter)

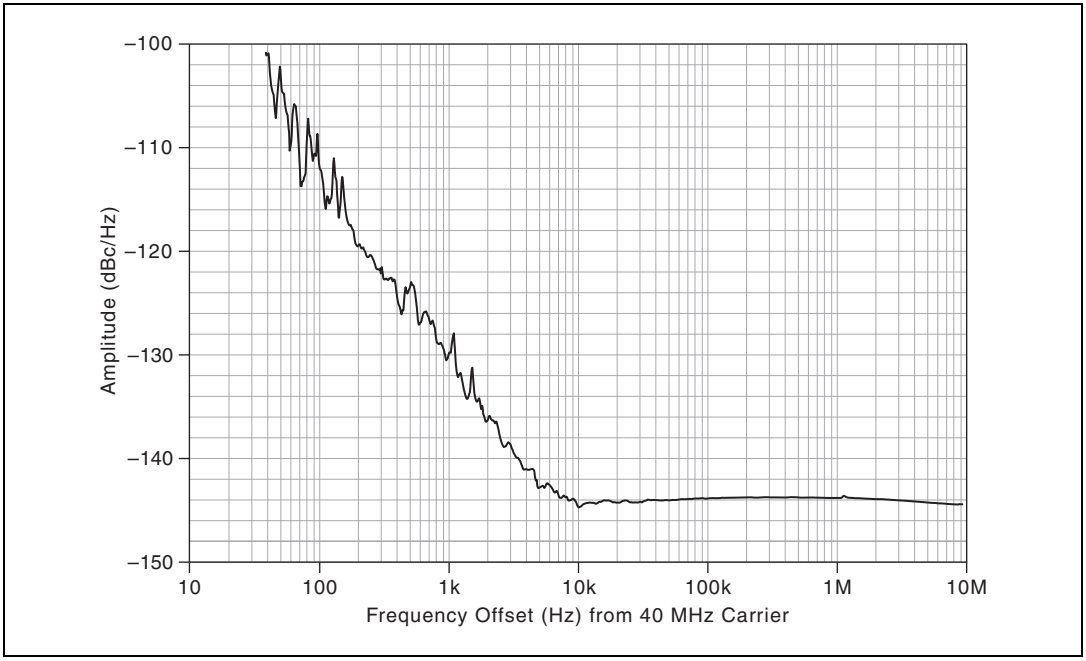


Figure 22. NI-5733/5734 AI Phase Noise (40 MHz Input, PLL Unlocked, Onboard Oscillator, 453 FS RMS Jitter)

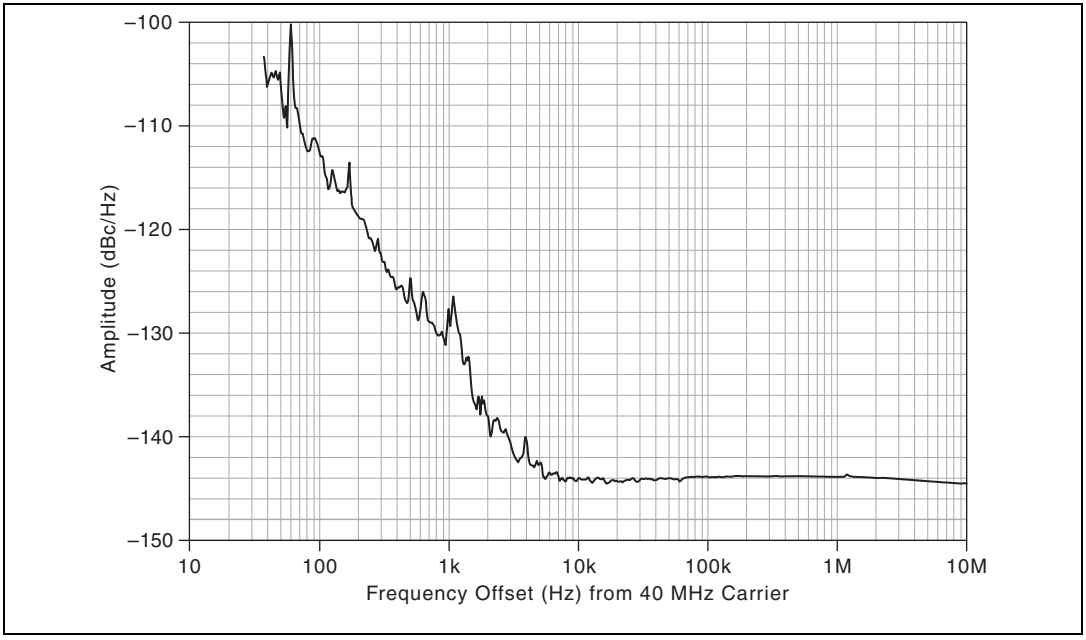


Figure 23. NI-5733/5734 AI Phase Noise
(40 MHz Input, PLL Locked to PXI 10 MHz Reference Clock, Onboard Oscillator, 448 FS RMS Jitter)

Terminated Spectral Measurements (16,382 point FFT, 30 Average RMS)

NI-5731

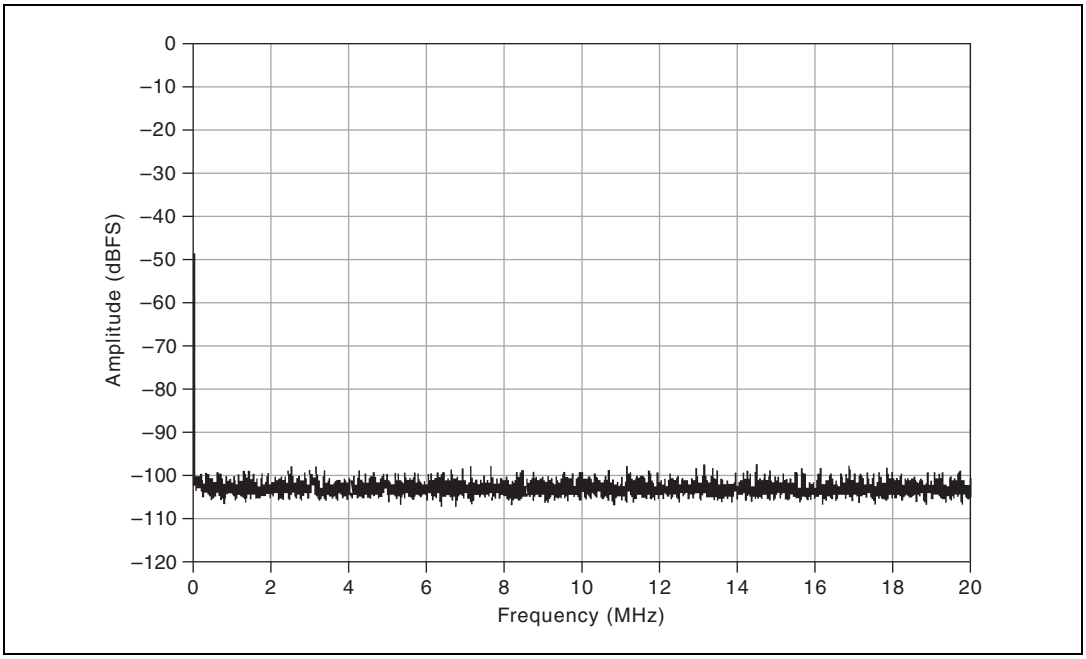


Figure 24. NI-5731 Gain at 0 dB; Elliptic, Bessel, or Filter Bypass; AC- or DC-coupled

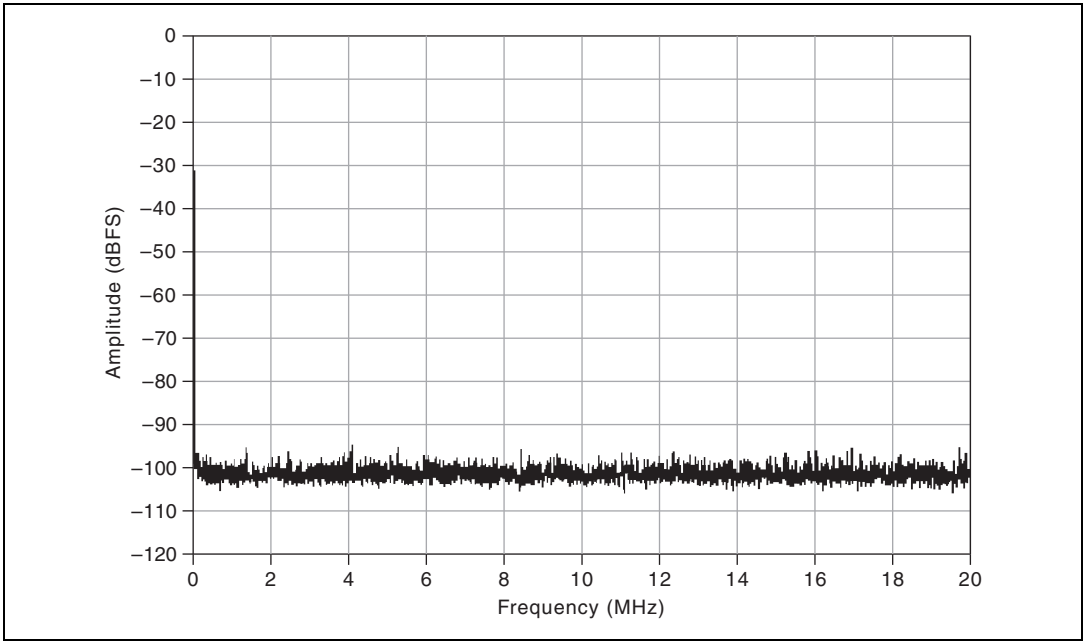


Figure 25. NI-5731 Gain at 12 dB; Elliptic, Bessel, or Filter Bypass; AC- or DC-coupled

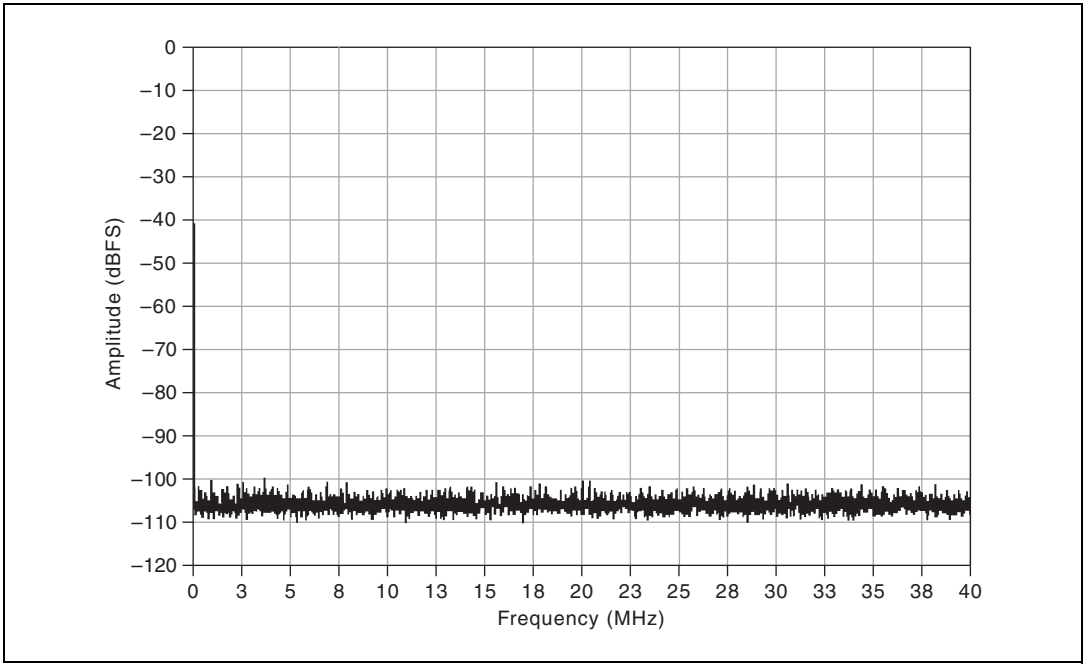


Figure 26. NI-5732 Gain at 0 dB; Elliptic, Bessel, or Filter Bypass; AC- or DC-coupled

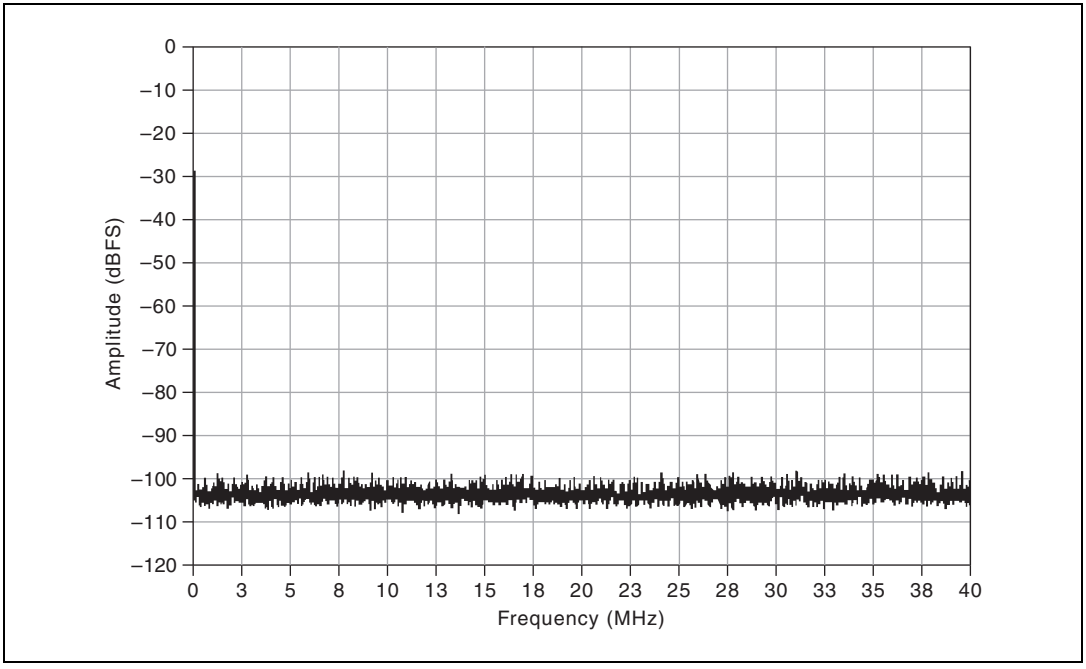


Figure 27. NI-5732 Gain at 12 dB; Elliptic, Bessel, or Filter Bypass; AC- or DC-coupled

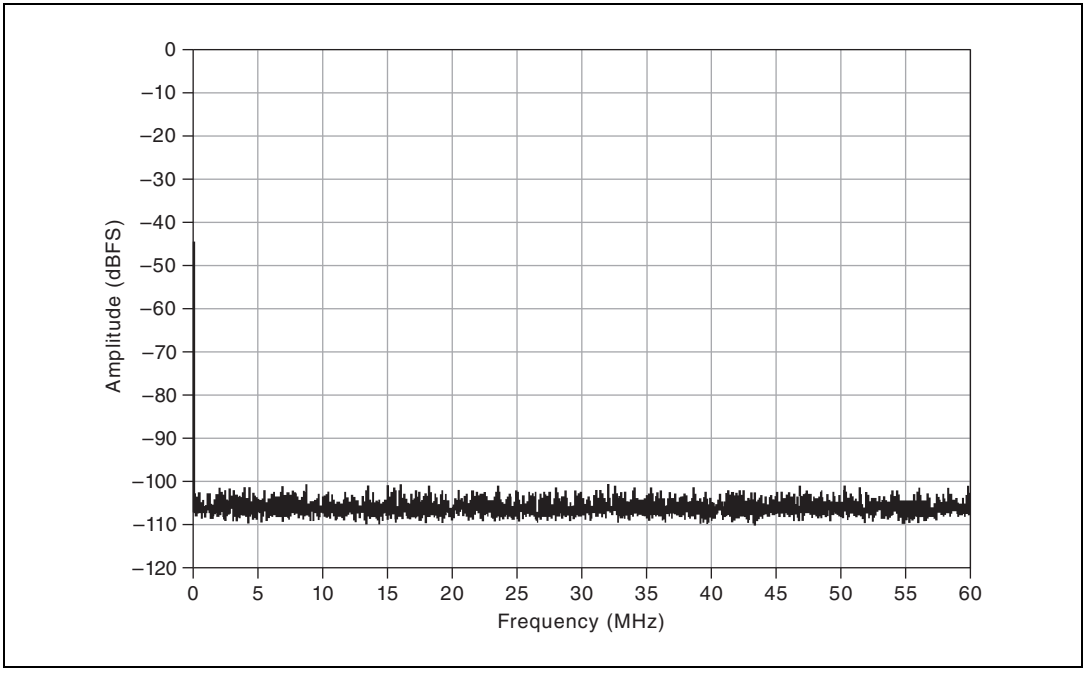


Figure 28. NI-5733/5734 Gain at 0 dB; Elliptic, Bessel, or Filter Bypass; AC- or DC-coupled

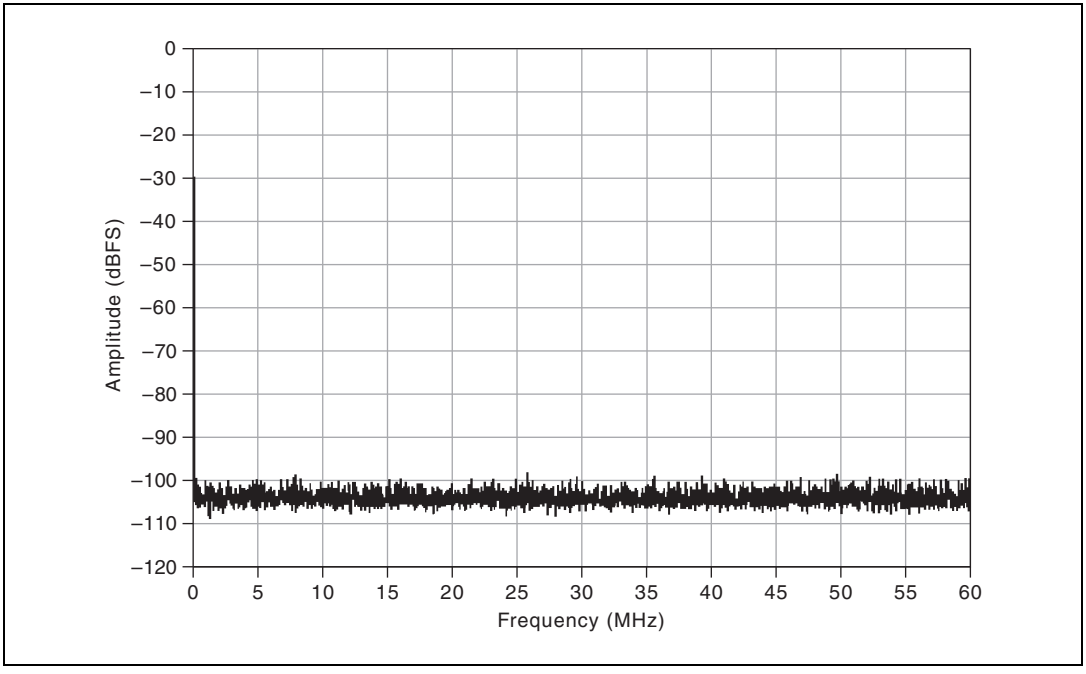


Figure 29. NI-5733/5734 Gain at 12 dB; Elliptic, Bessel, or Filter Bypass; AC- or DC-coupled

Spectral Measurements (16,382 point FFT)

NI-5731

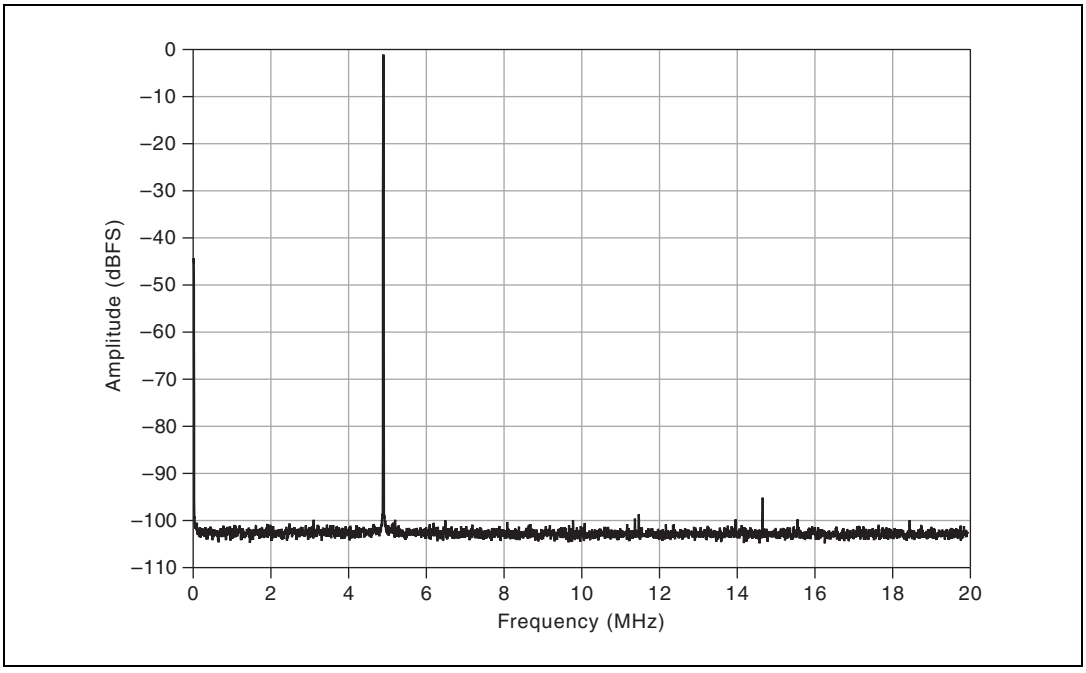


Figure 30. NI-5731 Gain at 0 dB: –1 dBFS at 4.9 MHz, –95 dBc SFDR, Bypass Filter, 100 Averages RMS

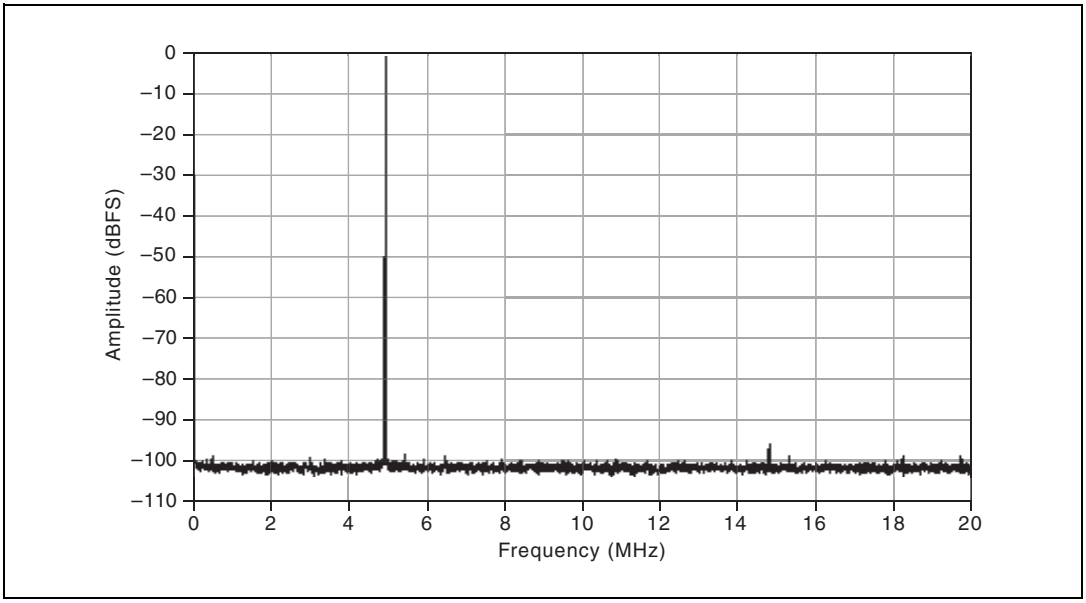


Figure 31. NI-5731 Gain at 12 dB: –1 dBFS at 4.9 MHz, –93 dBc SFDR, Bypass Filter, 100 Averages RMS

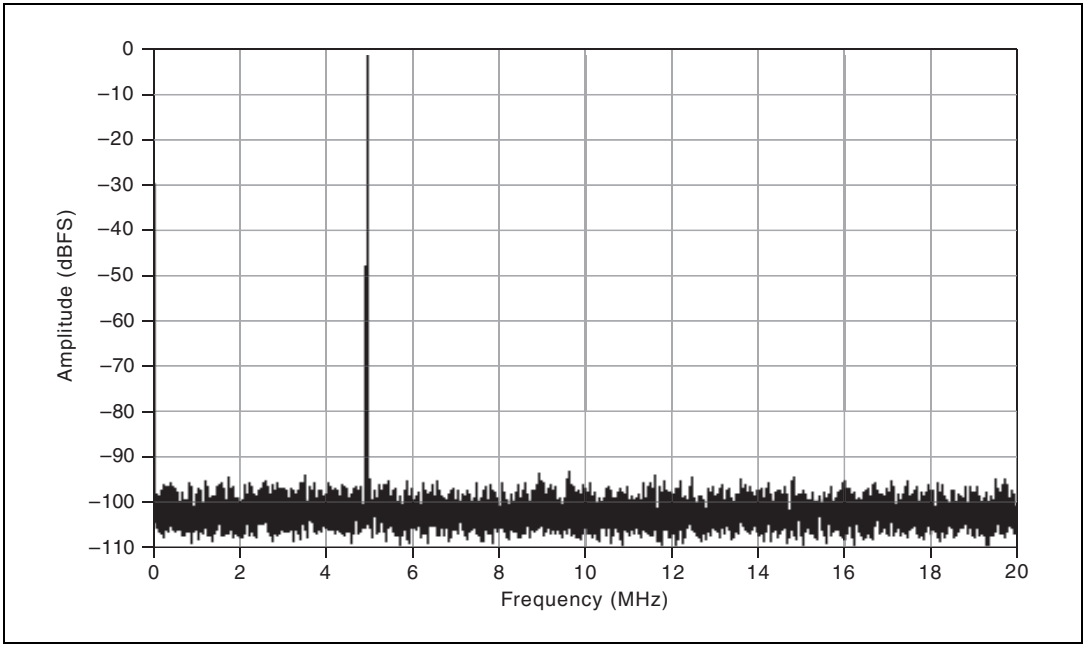


Figure 32. NI-5731 Gain at 12 dB: –1 dBFS at 4.9 MHz, –93 dBc SFDR, Bypass Filter, 10 Averages RMS

NI-5732

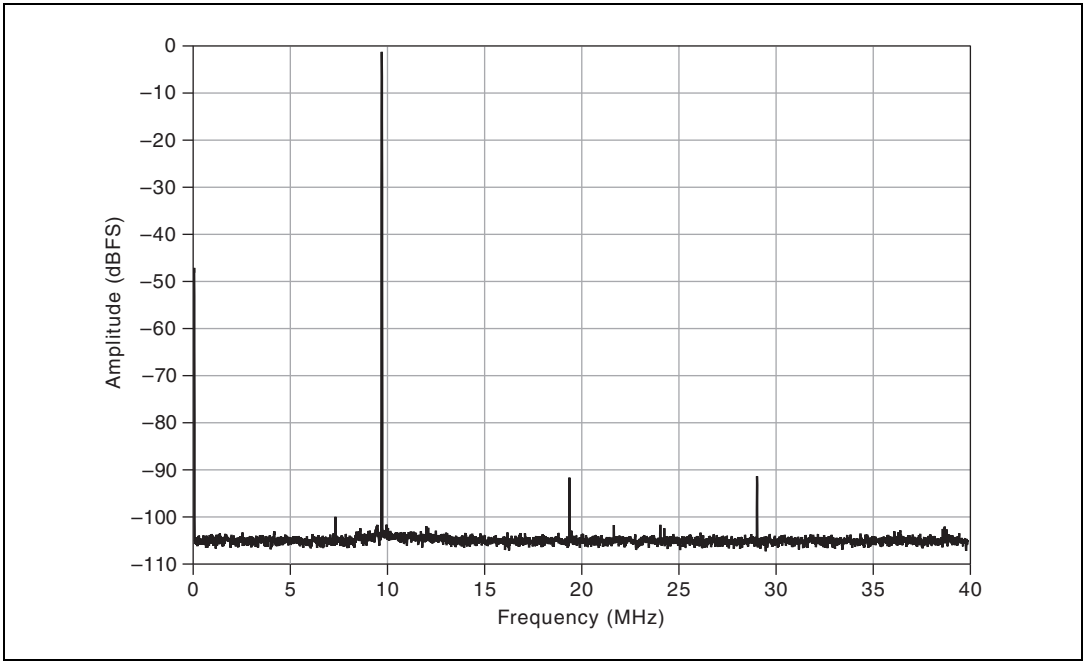


Figure 33. NI-5732 Gain at 0 dB: –1 dBFS at 9.7 MHz, –91 dBc SFDR, Bypass Filter, 100 Averages RMS

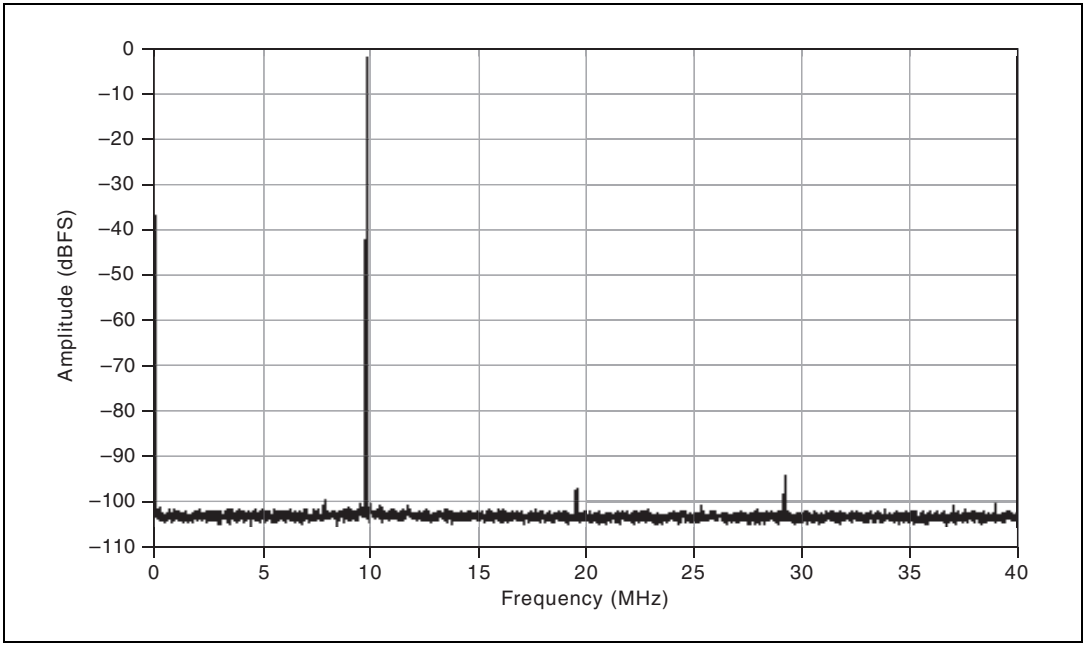


Figure 34. NI-5732 Gain at 12 dB: –1 dBFS at 9.7 MHz, –94 dBc SFDR, Bypass Filter, 100 Averages RMS

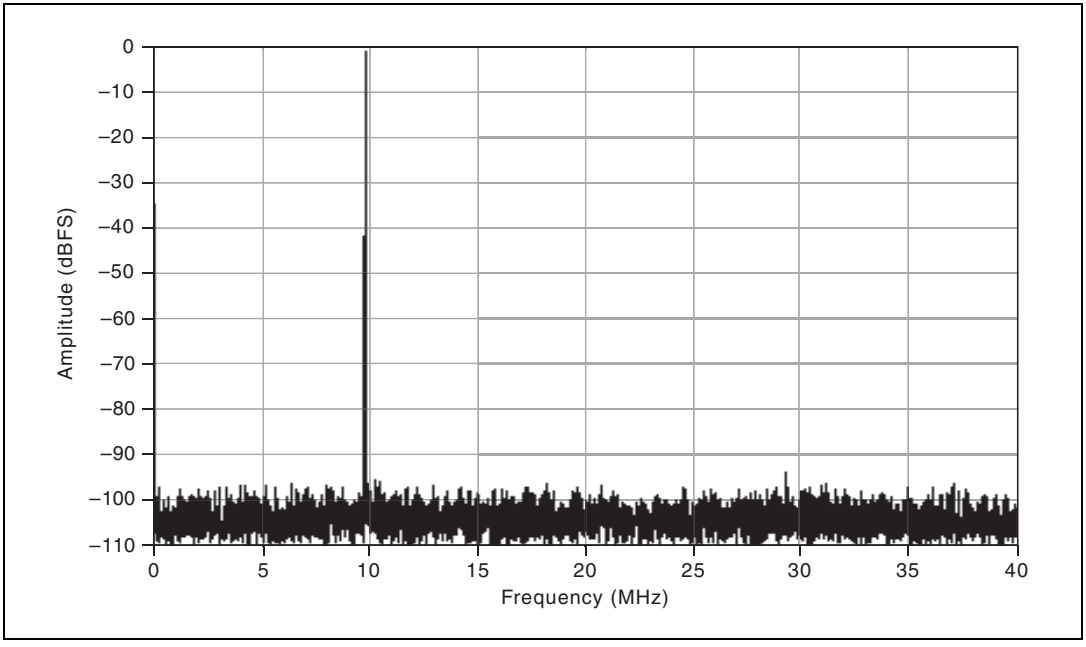


Figure 35. NI-5732 Gain at 12 dB: –1 dBFS at 9.7 MHz, –94 dBc SFDR, Bypass Filter, 10 Averages RMS

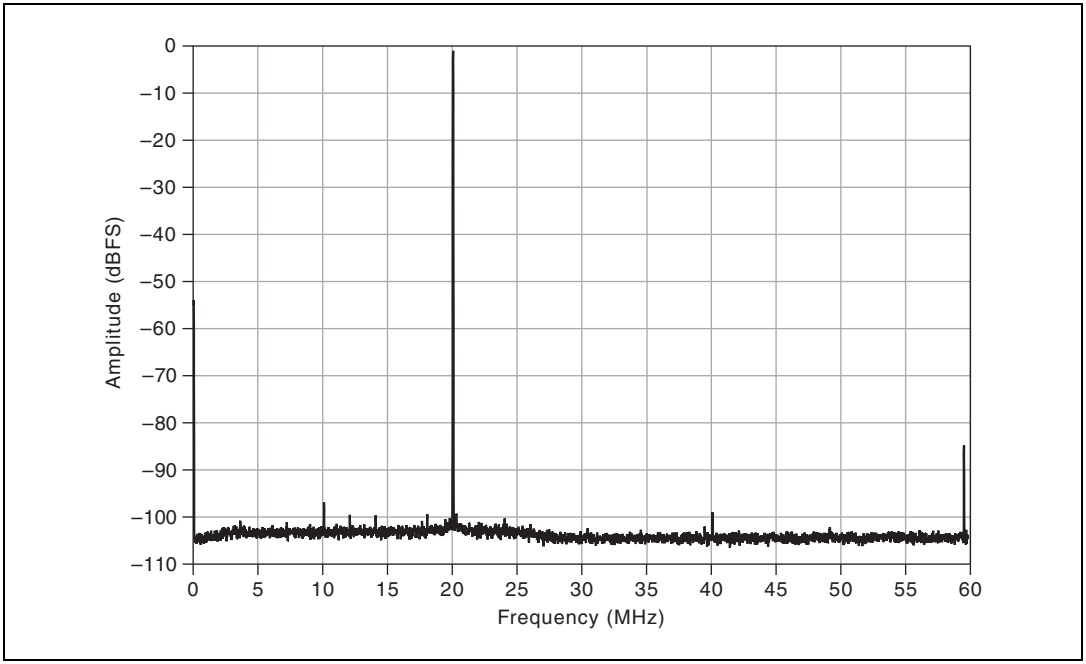


Figure 36. NI-5733/5734 Gain at 0 dB: –1 dBFS at 20.1 MHz, –85 dBc SFDR, Bypass Filter, 100 Averages RMS

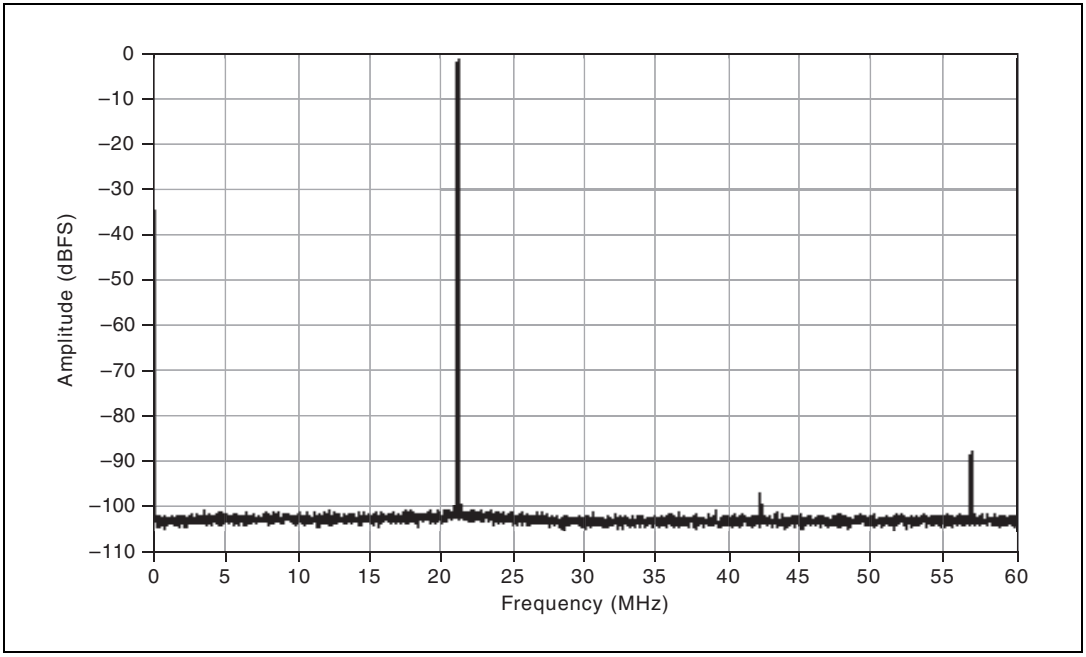


Figure 37. NI-5733/5734 Gain at 12 dB: –1 dBFS at 20.1 MHz, –87 dBc SFDR, Bypass Filter, 100 Averages RMS

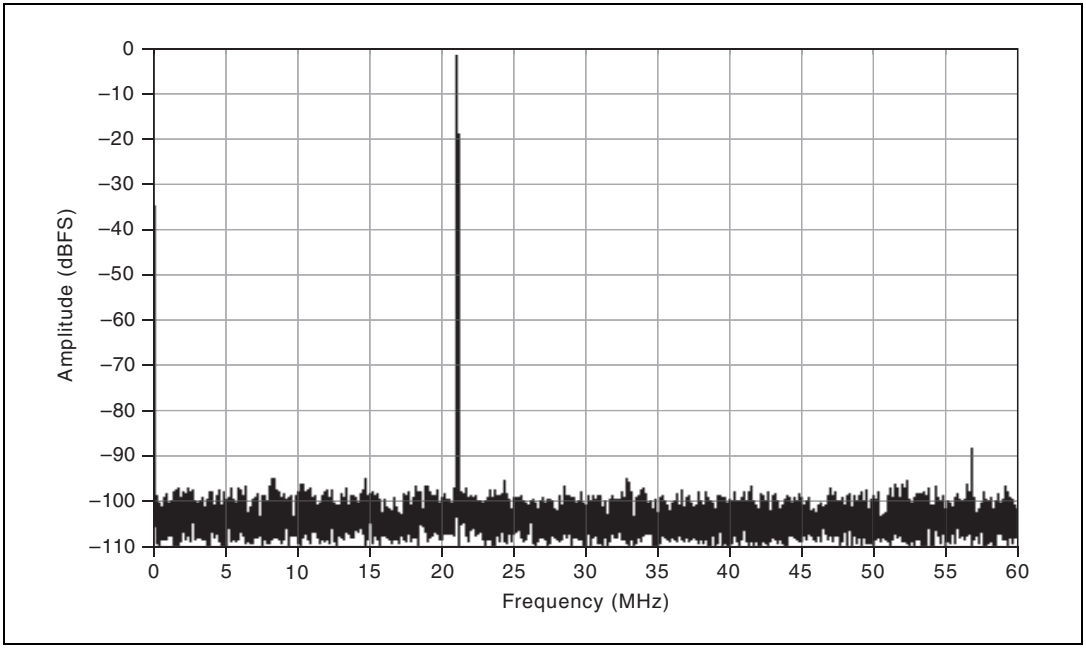


Figure 38. NI-5733/5734 Gain at 12 dB: –1 dBFS at 20.1 MHz, –87 dBc SFDR, Bypass Filter, 10 Averages RMS

Two-Tone FFT

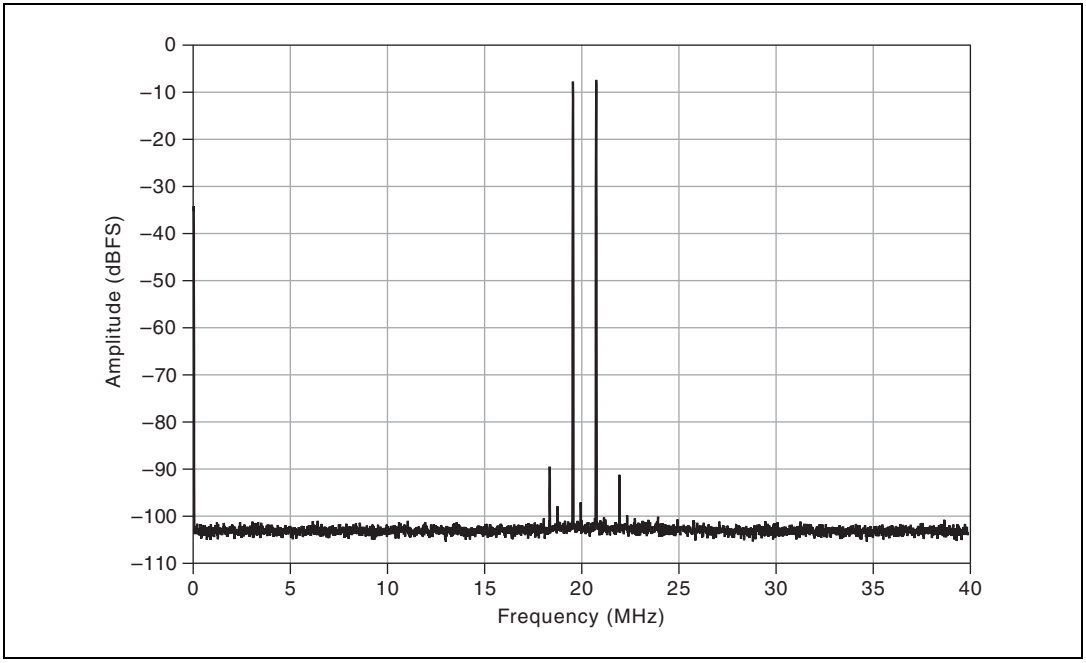


Figure 39. NI-5732 at 12 dB Gain and Filter Bypass: –83 dBc, f_{in} = 19.6 MHz (–7 dBFS), 20.8 MHz (–7 dBFS), 100 Average RMS

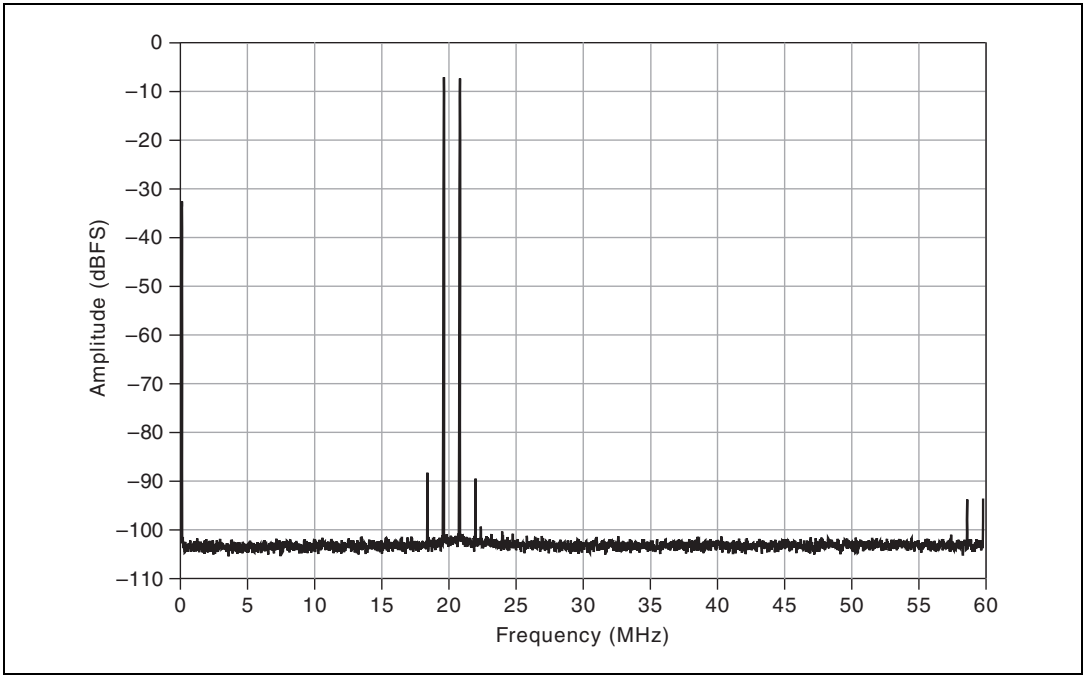


Figure 40. NI-5733/5734 at 12 dB Gain and Filter Bypass: –81 dBc, f_{in} = 19.6 MHz (–7 dBFS), 20.8 MHz

Internal Sample Clock

General Characteristics

Clock distribution part number.....AD9511[1]; clock distribution

Oscillator type.....VCXO

Frequency

- NI-5731.....40 MHz ± 50 ppm
- NI-5732.....80 MHz ± 100 ppm
- NI-5733/5734.....120 MHz ± 100 ppm

Phase noise.....Refer to the *Analog Input Total Phase Noise* section

Typical Specifications

Frequency stability

- Temperature .....±30 ppm over the operating temperature range
- Aging .....±5 ppm per year

CLK IN

General Characteristics

Number of channels.....1, single-ended

Connector type.....SMB

[1] For additional information about the AD9511, refer to the Analog Devices data sheet at `www.analog.com`.

Input impedance.....50 Ω

Input coupling .....AC

Input voltage range .....0.40 V_{pk-pk} to 5.2 V_{pk-pk}

Absolute maximum voltage .....±8.0 V DC, 8.0 V_{pk-pk} AC

Duty cycle .....40% to 60%

Table 15. NI-5731/5732/5733/5734 Clock Sources

Clock Configuration	Supported Sample Rates	External Clock Type	External Clock Frequency	Description
Internal Clock PLL Off	NI-5731 = 40 MS/s NI-5732 = 80 MS/s NI-5733 = 120 MS/s NI-5734 = 120 MS/s	—	—	The internal VCXO acts as a free-running clock.
Internal Clock PLL On (IoModSyncClk)	NI-5731 = 40 MS/s NI-5732 = 80 MS/s NI-5733 = 120 MS/s NI-5734 = 120 MS/s	—	10 MHz	The internal VCXO locks to IoModSyncClk (Sync Clock), which is provided only through the backplane of supported devices.
Internal Clock PLL On (CLK IN)	NI-5731 = 40 MS/s NI-5732 = 80 MS/s NI-5733 = 120 MS/s NI-5734 = 120 MS/s	Reference clock	10 MHz	The internal VCXO locks to an external Reference clock, which is provided through the CLK IN front panel connector.
External Clock (CLK IN)	The supported sample rate is equal to the external clock frequency.	Sample clock	NI-5731 Min = 3 MHz NI-5731 Max = 40 MHz NI-5732 Min = 20 MHz* NI-5732 Min = 10 MHz† NI-5732 Max = 80 MHz NI-5733 Min = 50 MHz NI-5733 Max = 120 MHz NI-5734 Min = 50 MHz NI-5734 Max = 120 MHz	An external Sample clock can be provided through the CLK IN front panel connector.

* Duty Cycle Stabilizer (DCS) enabled. DCS enabled is the default setting for all NI-5731/5732/5733/5734 CLIP items. You can disable the DCS by adjusting register 9 in the ADC.

† DCS disabled.

AUX I/O (Port 0 DIO <0..3>, Port 1 DIO <0..3>, and PFI <0..3>)

General Characteristics

Number of channels ..... 12 bidirectional (8 DIO and 4 PFI)

Connector type ..... HDMI

Interface standard ..... 3.3 V LVCMOS

Interface logic

- Maximum V_{IL} ..... 0.8 V
- Minimum V_{IH} ..... 2.0 V
- Maximum V_{OL} ..... 0.4 V
- Minimum V_{OH} ..... 2.7 V
- Maximum V_{OH} ..... 3.6 V
- Z_{out} ..... 50 Ω ± 20%
- I_{out} (DC) ..... ±2 mA

Pull-down resistor ..... 150 kΩ

Recommended operating voltage ..... –0.3 V to 3.6 V

Overvoltage protection ..... ±10 V

Maximum toggle frequency ..... 6.6 MHz

+5 V maximum power ..... 10 mA

+5 V voltage tolerance ..... 4.2 V to 5 V

Power

Total power, typical operation

- NI-5731 ..... 1.7 W
- NI-5732 ..... 2.1 W
- NI-5733 ..... 2.6 W
- NI-5734 ..... 4.5 W

Physical

Dimensions ..... 12.9 × 2.0 × 12.1 cm (5.1 × 0.8 × 4.7 in.)

Weight

- NI-5731/5732/5733 ..... 313 g (11.0 oz)
- NI-5734 ..... 332 g (11.7 oz)

Front panel connectors ..... BNC, SMB, and HDMI

Environmental

Operating environment[1] ..... 0 °C to 55 °C,
tested in accordance with IEC-60068-2-1 and IEC-60068-2-2.

Relative humidity range ..... 10% to 90%, noncondensing,
tested in accordance with IEC-60068-2-56.

Pollution Degree 2

Altitude ..... 2,000 m

Indoor use only.

Storage environment

Ambient temperature range ..... –20 °C to 70 °C,
tested in accordance with IEC-60068-2-1 and IEC-60068-2-2.

Relative humidity range ..... 5% to 95%, noncondensing,
tested in accordance with IEC-60068-2-56.

Note Clean the device with a soft, non-metallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.

Shock and Vibration

Operational shock ..... 30 g peak, half-sine, 11 ms pulse,
tested in accordance with IEC-60068-2-27.
Test profile developed in accordance with MIL-PRF-28800F.

Random vibration

Operating ..... 5 Hz to 500 Hz, 0.3 g_{rms}

Nonoperating ..... 5 Hz to 500 Hz, 2.4 g_{rms},
tested in accordance with IEC-60068-2-64.
Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.

Safety

This product meets the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

[1] For PXI/PXI Express chassis configurations that group NI FlexRIO adapter modules in three or more contiguous slots, NI recommends limiting the ambient operating temperature to less than 50 °C.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11) Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations and certifications, and additional information, refer to the *Online Product Certification* section of this document.

CE Compliance CE

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

To obtain product certifications and the Declaration of Conformity for this product, visit `ni.com/certification`, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *NI and the Environment* Web page at `ni.com/environment`. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, NI WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit `ni.com/environment/weee`.

电子信息产品污染控制管理办法 （中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 `ni.com/environment/rohs_china`。(For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)

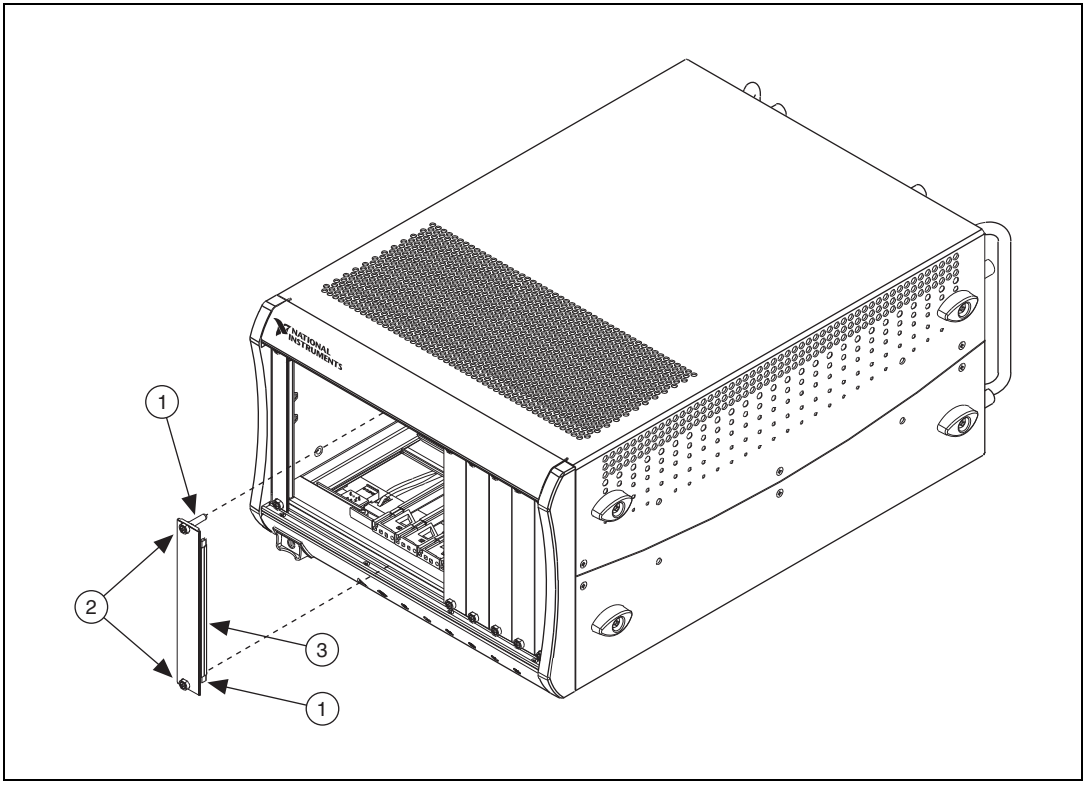
Appendix: Installing EMI Controls

To ensure specified EMC performance, an HDMI cable ferrite and PXI EMC filler panels must be properly installed in your NI FlexRIO system. Your kit includes the HDMI cable ferrite, but the PXI EMC filler panels (NI part number 778700-01) must be purchased separately. For more installation information, refer to the *NI FlexRIO FPGA Module Installation Guide and Specifications*.

Installing PXI EMC Filler Panels

Complete the following instructions to install PXI EMC filler panels (NI part number 778700-01) in your PXI chassis:

1. Remove the captive screw covers.
2. Install the PXI EMC filler panels by securing the captive mounting screws to the chassis, as shown in Figure 41. Make sure that the EMC gasket is on the right side of the PXI EMC filler panel.



1 Captive Screw Covers	2 Captive Mounting Screws	3 EMC Gasket

Figure 41. PXI EMC Filler Panels and Chassis

Note You must populate all slots with a module or a PXI EMC filler panel to ensure proper module cooling. Do not over tighten screws (2.5 lb-inch maximum). For additional information about the use of PXI EMC filler panels in your PXI system, visit `ni.com/info` and enter `emcpanels`.

Attaching an HDMI Cable Ferrite

Complete the following instructions to attach the snap-on cable ferrite included with your kit to your HDMI cable. Install the ferrite at the end of the HDMI cable nearest to the AUX I./O connector.

1. Open the ferrite by unsnapping the clasp.
2. Place the HDMI cable inside the ferrite.
3. Close the ferrite around the cable until it snaps into place.

NI Services

Visit `ni.com/support` to find support resources including documentation, downloads, and troubleshooting and application development self-help such as tutorials and examples.

Visit `ni.com/services` to learn about NI service offerings such as calibration options, repair, and replacement.

Visit `ni.com/register` to register your NI product. Product registration facilitates technical support and ensures that you receive important information updates from NI.

NI corporate headquarters is located at 11500 North Mopac Expressway, Austin, Texas, 78759-3504, USA.

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