

# SC Express

NI PXIe-4339 User Manual

*8 Ch, 24-bit, 25.6 kS/s Universal Bridge Input Module*

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# Getting Started

The NI PXIe-4339 has 24-bit resolution and supports sample rates from 1 S/s to 25.6 kS/s.

You can configure all settings on a per channel basis in software. The channels support the following features:

- Voltage and ratiometric (mV/V) measurements.
- Connecting sensors of all bridge configurations, including quarter-, half-, and full-bridge.
  - Quarter-bridge configurations are supported with the TB-4339/B/C.



**Note** For a complete list of terminal blocks supported by a specific release of NI-DAQmx, refer to the Readme, available on the version-specific download page or installation media.

- Balanced DC voltage excitation between 0.625 V and 10 V.
- Programmatic shunt calibration.
  - Shunt calibration resistors are provided on the TB-4339/B/C terminal blocks.
- Analog and digital filtering to reject out-of-band signals.
- Remote sense of bridge excitation.

## Installation

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Refer to the *NI PXIe-4339 and TB-4339/B/C Installation Guide and Terminal Block Specifications* for step-by-step software and hardware installation instructions.

## Module Specifications

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Refer to the *NI PXIe-4339 Specifications* document for module specifications.

## Module Accessories

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Refer to [ni.com/scexpress](http://ni.com/scexpress) for information about and a complete listing of supported accessories.



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# Using the Module

This chapter describes how to connect Wheatstone bridge sensors to the NI PXIe-4339 in quarter-, half-, and full-bridge configurations. It also provides the I/O connector signal pin assignments of the module.

Driver support for the NI PXIe-4339 was first available in NI-DAQmx 14.2. For the list of devices supported by a specific release, refer to the *NI-DAQmx Readme*, available on the version-specific download page or installation media.

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## Connecting Signals

This section includes a brief description of a general Wheatstone bridge and discusses how to connect the signals of supported strain-gage configuration types. It also discusses connecting leads for remote sensing and shunt calibration. Refer to the *NI PXIe-4339 and TB-4339/B/C Installation Guide and Terminal Block Specifications* for more signal connection information.

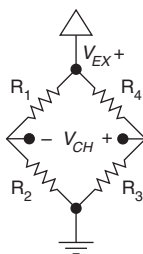
### Wheatstone Bridges

Many sensors, including strain-gages, load cells, pressure sensors, and torque sensors are based on the concept of a Wheatstone bridge. There are four elements, or legs, in a Wheatstone bridge. In general, these elements can be resistive or reactive, but in the majority of bridge based sensors, the elements are resistive. Most Wheatstone bridge based sensors use all four legs of the bridge as active sensing elements. However, common strain gage configurations include one, two or four active sensing elements. Figure 2-1 shows a resistive Wheatstone bridge circuit diagram.

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**Figure 2-1.** Basic Wheatstone Bridge Circuit Diagram

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The Wheatstone bridge is the electrical equivalent of two parallel voltage divider circuits.  $R_1$  and  $R_2$  compose one voltage divider circuit, and  $R_4$  and  $R_3$  compose the second voltage divider circuit. The output of a Wheatstone bridge is measured between the middle nodes of the two voltage dividers. A physical phenomena, such as a change in strain or temperature applied

to a specimen, changes the resistance of the sensing elements in the Wheatstone bridge, resulting in a bridge output voltage that is proportional to the physical phenomena. The output voltage of the bridge scales with the excitation voltage. However, the ratio of the bridge output ( $V_{CH}$ ) and the excitation voltage ( $V_{EX}$ ) remains fixed over variations in excitation voltage, and it is this unitless ratio ( $V_{CH}/V_{EX}$ ) that is of interest. To accurately measure the ratiometric output of a bridge based sensor, both the bridge output voltage ( $V_{CH}$ ) and the excitation voltage ( $V_{EX}$ ) must be known. Determination of the excitation voltage can be accomplished by either using an accurate voltage source or by measuring it. The NI PXIe-4339 uses circuitry that continuously measures the excitation voltage and applies it as a reference to its analog-to-digital converter (ADC). In this way the NI PXIe-4339 compensates for variations in the excitation voltage, and the module returns data as a ratio of the bridge output voltage to the excitation voltage.

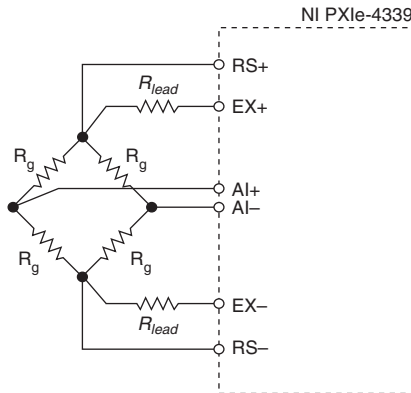
## Connection Options to Correct for Resistance Errors

The basic Wheatstone bridge in Figure 2-1 shows the excitation voltage impressed directly across the bridge. However, field wiring used to connect sensors to measurement devices have a non-zero resistance, and this resistance can create errors in bridge circuit measurements. The NI PXIe-4339 provides two mechanisms to correct for these errors: remote sensing and shunt calibration.

### Remote Sensing

Remote sensing continuously and automatically corrects for errors in excitation leads, and generally is most appropriate for half- and full-bridge sensors. Moreover, its use is most critical in applications that employ long wires and/or small gauge wires, as these have higher resistance. The resistance in the wires that connect the excitation voltage to the bridge causes a voltage drop, which is a source of gain error. The NI PXIe-4339 includes remote sensing to compensate for this gain error. Connect remote sense inputs of the NI PXIe-4339 to the excitation voltage wires of the sensor as close to the bridge circuit as possible. Refer to the full-bridge diagram in Figure 2-2 for an illustration of how to connect remote sense wires.

**Figure 2-2.** Connecting Remote Sense Wires to the NI PXIe-4339



The actual bridge excitation voltage measured at the bridge is smaller than the voltage sourced at the EX+ and EX- connector pins. This reduction in voltage is due to the voltage drop across the excitation lead wire resistance ( $R_{lead}$ ). If you do not use remote sensing of the actual bridge voltage, the resulting reduction in gain is given by the following equations:

- for half-bridge sensors  $\frac{R_{lead}}{R_g}$
- for full-bridge sensors  $\frac{2 \times R_{lead}}{R_g}$

If you connect the remote sense signals directly to the bridge resistors, the NI PXIe-4339 senses the actual bridge voltage using high-impedance RS leads and eliminates the gain errors caused by the resistance of the EX+ and EX- leads.

## Shunt Calibration

Shunt calibration can correct for errors from the resistance of both the excitation wiring and wiring in the individual resistors of the bridge. While remote sensing only corrects for resistances from the EX leads on the NI PXIe-4339 to the sensor, shunt calibration corrects for these errors and for errors caused by wire resistance within an arm of the bridge. Shunt calibration is most useful with three-wire quarter-bridge sensors because there may be significant resistance in the wiring to the sensor and remote sense can not be used. Refer to Figure 2-4 for a diagram of this setup. The NI PXIe-4339 shunt calibration circuitry consists of a software-controlled switch that is used in conjunction with the shunt calibration resistors provided on the TB-4339/B/C terminal blocks. Refer to the software help for information about enabling the shunt calibration resistors on the NI PXIe-4339. Shunt calibration involves simulating the input of a gage by changing the resistance of an arm in the bridge by some known amount. This is accomplished by shunting, or connecting, a large resistor of known value across one arm of the bridge, creating a known change in the bridge output. This change is then measured and compared to the expected bridge output. The result can be used to correct gain errors in the entire measurement path or to simply verify general operation in the setup.

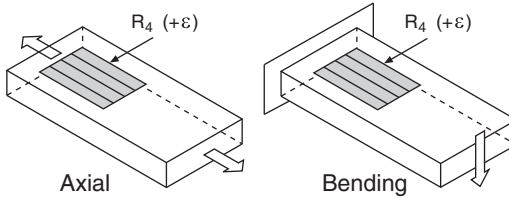
# Strain Gage Sensor Configurations

This section describes the configurations and signal connection of various supported strain-gage configuration types.

## Quarter-Bridge Type I

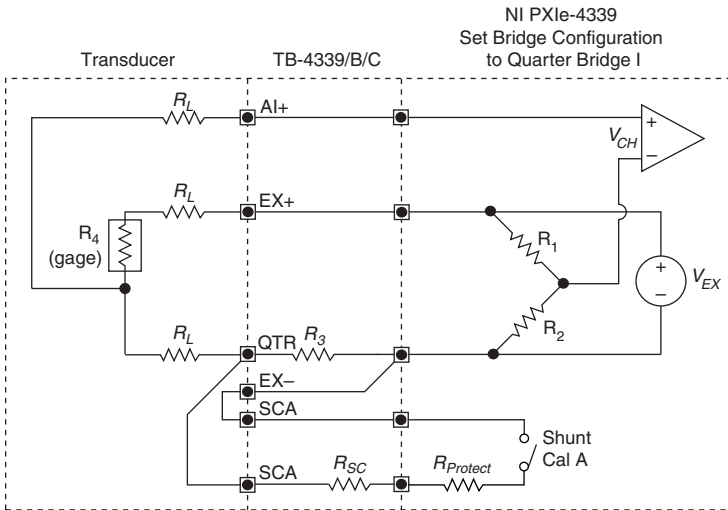
This section provides information for the quarter-bridge strain-gage configuration type I. The quarter-bridge type I measures either axial or bending strain. Figure 2-3 shows how to position a strain-gage resistor in an axial and bending configuration. Figure 2-4 shows the quarter-bridge type I circuit wiring diagram.

**Figure 2-3. Quarter-Bridge Type I Measuring Axial and Bending Strain**



A quarter-bridge type I configuration has the following characteristics:

- A single active strain-gage element is mounted in the principal direction of axial or bending strain.
- A passive quarter-bridge completion resistor ( $R_3$ ) is required in addition to half-bridge completion resistors ( $R_1$  and  $R_2$ ).
- Half-bridge completion resistors ( $R_1$  and  $R_2$ ) are provided by the NI PXIe-4339 module.
- The quarter-bridge completion resistor ( $R_3$ ) is provided on the TB-4339/B/C terminal blocks.
- The shunt calibration resistor ( $R_{SC}$ ) is provided on the TB-4339/B/C terminal blocks.
- The Shunt Cal A switch is provided on the NI PXIe-4339 module.
- Sensitivity  $\sim 0.5 \mu\text{V}/\text{V}$  per  $\mu\epsilon$ , for  $GF = 2.0$ .

**Figure 2-4. Quarter-Bridge I Circuit Diagram**

The following symbols apply to the circuit diagram and equations:

- $R_1$  and  $R_2$ —Half-bridge completion resistors located inside the NI PXIe-4339.
- $R_3$ —Quarter-bridge completion resistor located inside the TB-4339/B/C.  
 $R_3$  must be equal to the nominal resistance of the active gage ( $R_4$ ).
- $R_{SC}$ —Shunt calibration resistor located inside the TB-4339/B/C.
- $R_4$ —Active element measuring tensile strain ( $+\epsilon$ ). You provide this element.
- $R_L$ —Lead resistance. The resistance in the EX+ and QTR field wiring should match.
- $GF$ —Gage Factor, specified by the gage manufacturer.
- $V_{CH}$ —Measured voltage of the bridge.
- $V_{EX}$ —Excitation voltage provided by the NI PXIe-4339.
- $R_{Protect}$ —10 k $\Omega$  resistor in series with the Shunt Cal A switch to protect against external fault voltages. The total shunt cal resistance is equal to the  $R_{SC}$  and  $R_{Protect}$  series combination.
- $V_r$ —Offset compensated ratiometric bridge output defined by the following equation:

$$V_r = \left( \frac{V_{CH}(\text{strained}) - V_{CH}(\text{unstrained})}{V_{EX}} \right)$$



**Note** The ratio of the bridge output voltage and the excitation voltage is done internally on the NI PXIe-4339.

To convert module readings to strain use the following equation:

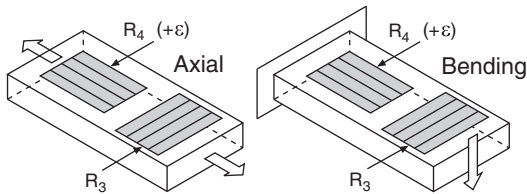
$$strain(\epsilon) = \frac{-4V_r}{GF(1 + 2V_r)}$$

To compensate for lead resistance errors, use shunt calibration.

## Quarter-Bridge Type II

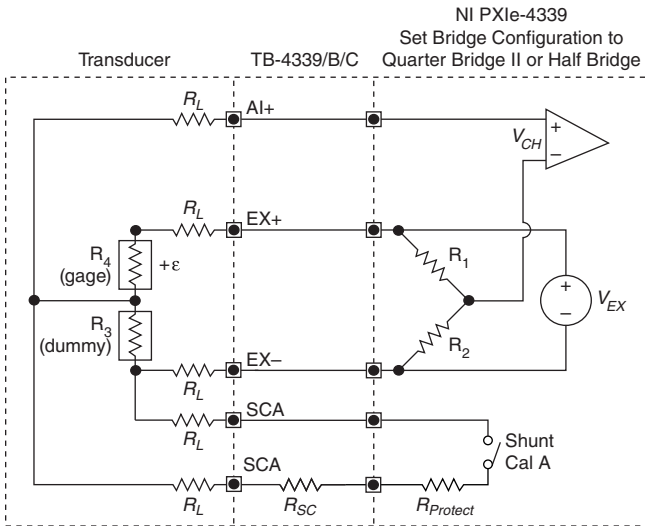
This section provides information for the quarter-bridge strain-gage configuration type II. The quarter-bridge type II configuration measures either axial or bending strain. Figure 2-5 shows how to position a strain-gage resistor in an axial and bending configurations. Figure 2-6 shows the quarter-bridge type II circuit wiring diagram.

**Figure 2-5. Quarter-Bridge Type II Measuring Axial and Bending Strain**



A quarter-bridge type II has the following characteristics:

- One active strain-gage element and one passive quarter-bridge element (dummy gage) used for temperature compensation. The active element ( $R_4$ ) is mounted in the direction of axial or bending strain. The dummy gage ( $R_3$ ) is mounted in close thermal contact with the strain specimen but not bonded to the specimen, and is usually mounted perpendicular to the principal axis of strain.
- Completion resistors ( $R_1$  and  $R_2$ ) provide half-bridge completion. These resistors are provided by the NI PXIe-4339 module.
- Sensitivity  $\sim 0.5 \mu\text{V/V}$  per  $\mu\epsilon$ , for  $GF = 2.0$ .

**Figure 2-6. Quarter-Bridge II Circuit Diagram**


The following symbols apply to the circuit diagram and equations:

- $R_1$  and  $R_2$ —Half-bridge completion resistors located inside the NI PXIe-4339.
- $R_3$ —Quarter-bridge completion resistor located in close proximity to the active gage.  
 $R_3$  must be equal to the nominal resistance of the active gage ( $R_4$ ).
- $R_{SC}$ —Shunt calibration resistor located inside the TB-4339/B/C.
- $R_4$ —Active element measuring tensile strain ( $+\epsilon$ ).
- $R_L$ —Lead resistance.
- $GF$ —Gage Factor, specified by the gage manufacturer.
- $V_{CH}$ —Measured voltage of the bridge.
- $V_{EX}$ —Excitation voltage provided by the NI PXIe-4339.
- $R_{Protect}$ —10 k $\Omega$  resistor in series with the Shunt Cal A switch to protect against external fault voltages. The total shunt cal resistance is equal to the  $R_{SC}$  and  $R_{Protect}$  series combination.
- $V_r$ —Offset compensated ratiometric bridge output defined by the following equation:

$$V_r = \left( \frac{V_{CH}(\text{strained}) - V_{CH}(\text{unstrained})}{V_{EX}} \right)$$



**Note** The ratio of the bridge output voltage and the excitation voltage is done internally on the NI PXIe-4339.

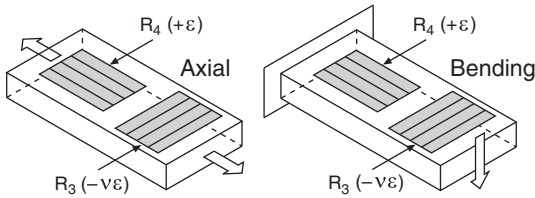
To convert module readings to strain use the following equation:

$$strain(\epsilon) = \frac{-4V_r}{GF(1 + 2V_r)}$$

## Half-Bridge Type I

This section provides information for the half-bridge strain-gage configuration type I. The half-bridge type I measures either axial or bending strain. Figure 2-7 shows how to position strain-gage resistors in an axial and bending configurations. Figure 2-8 shows the half-bridge type I circuit wiring diagram.

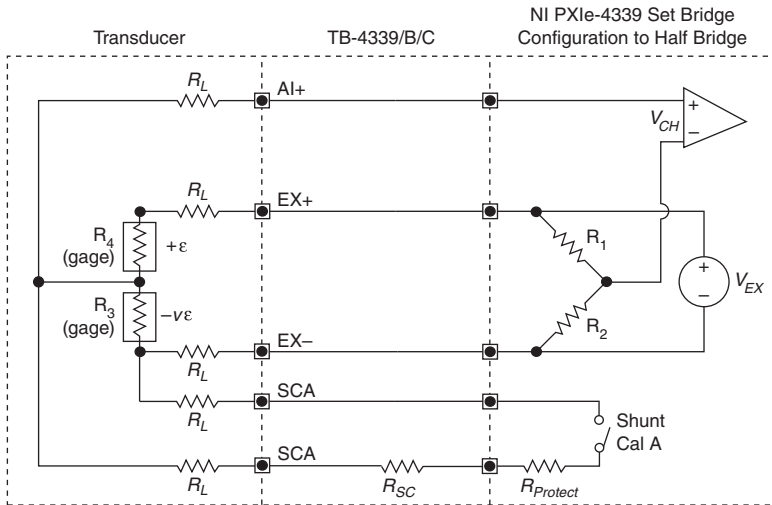
**Figure 2-7. Half-Bridge Type I Measuring Axial and Bending Strain**



A half-bridge type I has the following characteristics:

- Two active strain-gage elements. One strain-gage element is mounted in the direction of axial strain while the other acts as a Poisson gage and is mounted perpendicular to the principal axis of strain.
- Half-bridge completion resistors ( $R_1$  and  $R_2$ ) are provided by the NI PXIe-4339.
- Sensitive to both axial and bending strain.
- Sensitivity  $\sim 0.65 \mu\text{V/V}$  per  $\mu\epsilon$ , for  $GF = 2.0$ .



**Figure 2-8. Half-Bridge Type I Circuit Diagram**

The following symbols apply to the circuit diagram and equations:

- $R_1$  and  $R_2$ —Half-bridge completion resistors located inside the NI PXIe-4339.
- $R_3$ —Active element measuring compression from Poisson effect ( $-v\epsilon$ ).
- $R_{SC}$ —Shunt calibration resistor located inside the TB-4339/B/C.
- $R_4$ —Active element measuring tensile strain ( $+\epsilon$ ).
- $R_L$ —Lead resistance.
- $GF$ —Gage Factor, specified by the gage manufacturer.
- $v$ —Poisson's ratio, defined as the negative ratio of transverse strain to axial strain (longitudinal) strain. Poisson's ratio is a material property of the specimen you are measuring.
- $V_{CH}$ —Measured voltage of the bridge.
- $V_{EX}$ —Excitation voltage provided by the NI PXIe-4339.
- $R_{Protect}$ —10 k $\Omega$  resistor in series with the Shunt Cal A switch to protect against external fault voltages. The total shunt cal resistance is equal to the  $R_{SC}$  and  $R_{Protect}$  series combination.
- $V_r$ —Offset compensated ratiometric bridge output defined by the following equation:

$$V_r = \left( \frac{V_{CH}(\text{strained}) - V_{CH}(\text{unstrained})}{V_{EX}} \right)$$



**Note** The ratio of the bridge output voltage and the excitation voltage is done internally on the NI PXIe-4339.

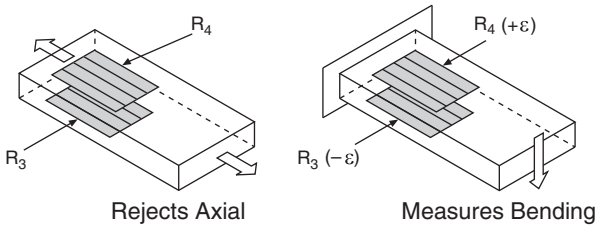
To convert module readings to strain use the following equation:

$$strain(\epsilon) = \frac{-4V_r}{GF[(1 + \nu) - 2V_r(\nu - 1)]}$$

## Half-Bridge Type II

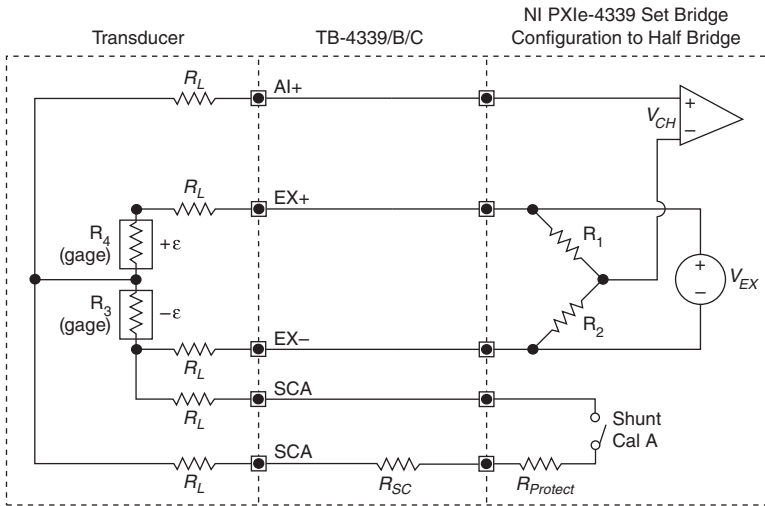
This section provides information for the half-bridge strain-gage configuration type II. The half-bridge type II only measures bending strain. Figure 2-9 shows how to position strain-gage resistors in a bending configuration. Figure 2-10 shows the half-bridge type II circuit wiring diagram.

**Figure 2-9.** Half-Bridge Type II Rejecting Axial and Measuring Bending Strain



A half-bridge type II configuration has the following characteristics:

- Two active strain-gage elements. One strain-gage element is mounted in the direction of bending strain on one side of the strain specimen (top) while the other is mounted in the direction of bending strain on the opposite side (bottom).
- Half-bridge completion resistors ( $R_1$  and  $R_2$ ) are provided by the NI PXIe-4339.
- Sensitive to bending strain.
- Rejects axial strain.
- Sensitivity  $\sim 1 \mu\text{V/V}$  per  $\mu\epsilon$ , for  $GF = 2.0$ .

**Figure 2-10.** Half-Bridge Type II Circuit Diagram

The following symbols apply to the circuit diagram and equations:

- $R_1$  and  $R_2$ —Half-bridge completion resistors located inside the NI PXIe-4339.
- $R_3$ —Active element measuring compressive strain ( $-\epsilon$ ).
- $R_{SC}$ —Shunt calibration resistor located inside the TB-4339/B/C.
- $R_4$ —Active element measuring tensile strain ( $+\epsilon$ ).
- $R_L$ —Lead resistance.
- $GF$ —Gage Factor, specified by the gage manufacturer.
- $V_{CH}$ —Measured voltage of the bridge.
- $V_{EX}$ —Excitation voltage provided by the NI PXIe-4339.
- $R_{protect}$ —10 k $\Omega$  resistor in series with the Shunt Cal A switch to protect against external fault voltages. The total shunt cal resistance is equal to the  $R_{SC}$  and  $R_{protect}$  series combination.
- $V_r$ —Offset compensated ratiometric bridge output defined by the following equation:

$$V_r = \left( \frac{V_{CH}(\text{strained}) - V_{CH}(\text{unstrained})}{V_{EX}} \right)$$



**Note** The ratio of the bridge output voltage and the excitation voltage is done internally on the NI PXIe-4339.

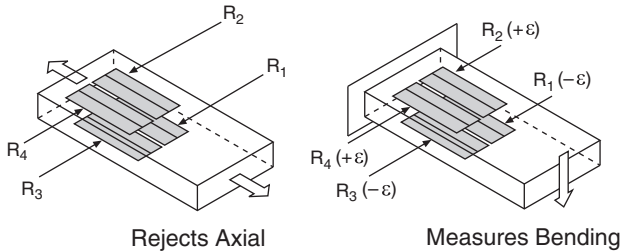
To convert module readings to strain use the following equation:

$$\text{strain } (\epsilon) = \frac{-2V_r}{GF}$$

## Full-Bridge Type I

This section provides information for the full-bridge strain-gage configuration type I. The full-bridge type I only measures bending strain. Figure 2-11 shows how to position strain-gage resistors in a bending configuration. Figure 2-12 shows the full-bridge type I circuit wiring diagram.

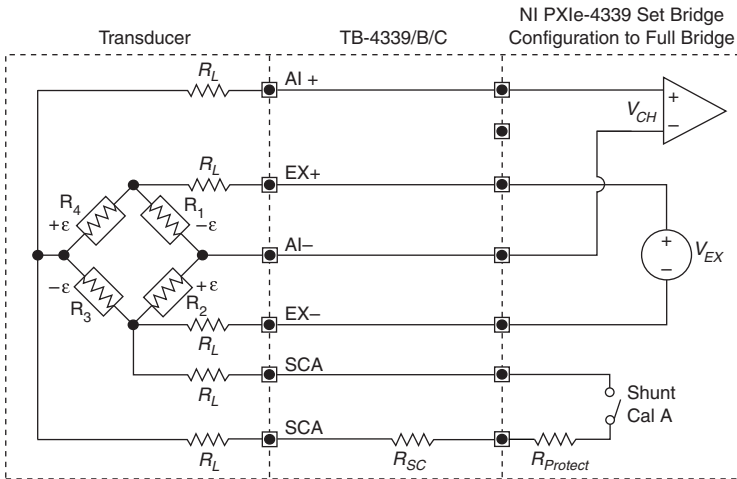
**Figure 2-11.** Full-Bridge Type I Rejecting Axial and Measuring Bending Strain



A full-bridge type I configuration has the following characteristics:

- Four active strain-gage elements. Two strain-gage elements are mounted in the direction of bending strain on one side of the strain specimen (top) while the other two are mounted in the direction of bending strain on the opposite side (bottom).
- Highly sensitive to bending strain.
- Rejects axial strain.
- Sensitivity  $\sim 2 \mu\text{V/V}$  per  $\mu\epsilon$ , for  $GF = 2.0$ .

Figure 2-12. Full-Bridge Type I Circuit Diagram



The following symbols apply to the circuit diagram and equations:

- $R_1$ —Active element measuring compressive strain ( $-\epsilon$ ).
- $R_2$ —Active element measuring tensile strain ( $+\epsilon$ ).
- $R_3$ —Active element measuring compressive strain ( $-\epsilon$ ).
- $R_4$ —Active element measuring tensile strain ( $+\epsilon$ ).
- $R_{SC}$ — Shunt calibration resistor located inside the TB-4339/B/C.
- $R_L$ —Lead resistance.
- $GF$ —Gage Factor, specified by the gage manufacturer.
- $V_{CH}$ —Measured voltage of the bridge.
- $V_{EX}$ —Excitation voltage provided by the NI PXIe-4339.
- $R_{Protect}$ —10 k $\Omega$  resistor in series with the Shunt Cal A switch to protect against external fault voltages. The total shunt cal resistance is equal to the  $R_{SC}$  and  $R_{Protect}$  series combination.
- $V_r$ —Offset compensated ratiometric bridge output defined by the following equation:

$$V_r = \left( \frac{V_{CH}(\text{strained}) - V_{CH}(\text{unstrained})}{V_{EX}} \right)$$



**Note** The ratio of the bridge output voltage and the excitation voltage is done internally on the NI PXIe-4339.

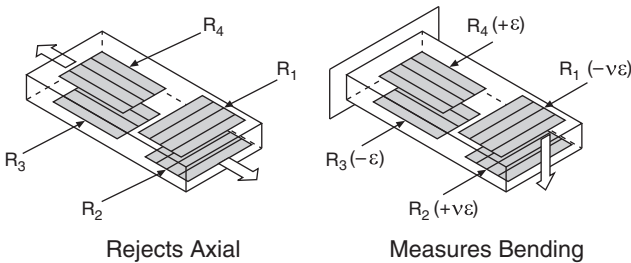
To convert module readings to strain use the following equation:

$$strain (\epsilon) = \frac{-V_r}{GF}$$

## Full-Bridge Type II

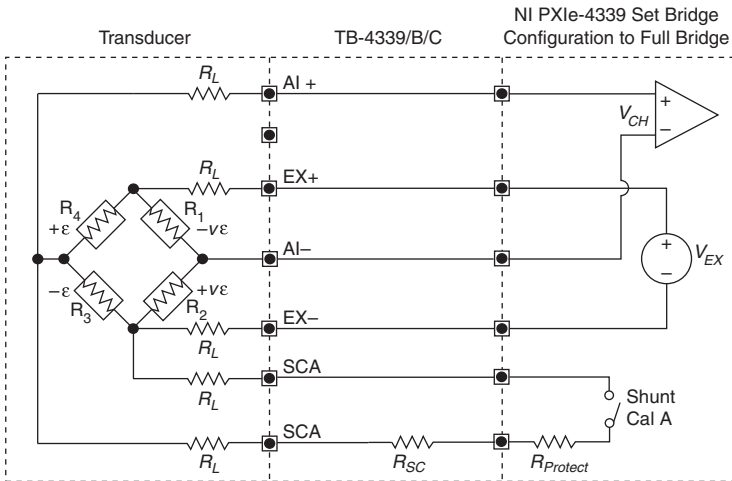
This section provides information for the full-bridge type II strain-gage configuration. The full-bridge type II only measures bending strain. Figure 2-13 shows how to position strain-gage resistors in a bending configuration. Figure 2-14 shows the full-bridge type II circuit wiring diagram.

**Figure 2-13. Full-Bridge Type II Rejecting Axial and Measuring Bending Strain**



A full-bridge type II configuration has the following characteristics:

- Four active strain-gage elements. Two are mounted in the direction of bending strain with one on one side of the strain specimen (top) and the other on the opposite side (bottom). The other two act together as a Poisson gage and are mounted transverse (perpendicular) to the principal axis of strain with one on one side of the strain specimen (top) and the other on the opposite side (bottom).
- Rejects axial strain.
- Sensitivity  $\sim 1.3 \mu\text{V/V}$  per  $\mu\epsilon$ , for  $GF = 2.0$ .

**Figure 2-14.** Full-Bridge Type II Circuit Diagram

The following symbols apply to the circuit diagram and equations:

- $R_1$ —Active element measuring compressive Poisson effect ( $-v\epsilon$ ).
- $R_2$ —Active element measuring tensile Poisson effect ( $+v\epsilon$ ).
- $R_3$ —Active element measuring compressive strain ( $-\epsilon$ ).
- $R_4$ —Active element measuring tensile strain ( $+\epsilon$ ).
- $R_{SC}$ — Shunt calibration resistor located inside the TB-4339/B/C.
- $R_L$ — Lead resistance.
- $GF$ —Gage Factor, specified by the gage manufacturer.
- $\nu$ —Poisson's ratio, defined as the negative ratio of transverse strain to axial strain (longitudinal) strain. Poisson's ratio is a material property of the specimen you are measuring.
- $V_{CH}$ —Measured voltage of the bridge.
- $V_{EX}$ —Excitation voltage provided by the NI PXIe-4339.
- $R_{Protect}$ —10 k $\Omega$  resistor in series with the Shunt Cal A switch to protect against external fault voltages. The total shunt cal resistance is equal to the  $R_{SC}$  and  $R_{Protect}$  series combination.
- $V_r$ —Offset compensated ratiometric bridge output defined by the following equation:

$$V_r = \left( \frac{V_{CH}(\text{strained}) - V_{CH}(\text{unstrained})}{V_{EX}} \right)$$



**Note** The ratio of the bridge output voltage and the excitation voltage is done internally on the NI PXIe-4339.

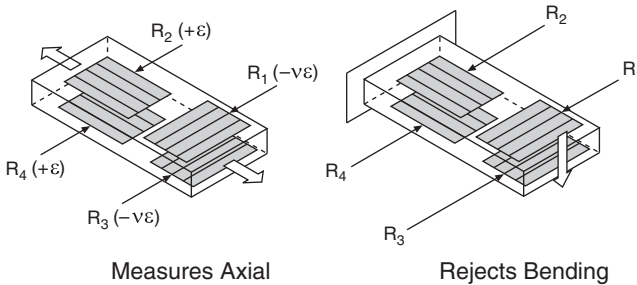
To convert module readings to strain use the following equation:

$$strain(\epsilon) = \frac{-2V_r}{GF(1 + \nu)}$$

### Full-Bridge Type III

This section provides information for the full-bridge strain-gage configuration type III. The full-bridge type III only measures axial strain. Figure 2-15 shows how to position strain-gage resistors in an axial configuration. Figure 2-16 shows the full-bridge type III circuit wiring diagram.

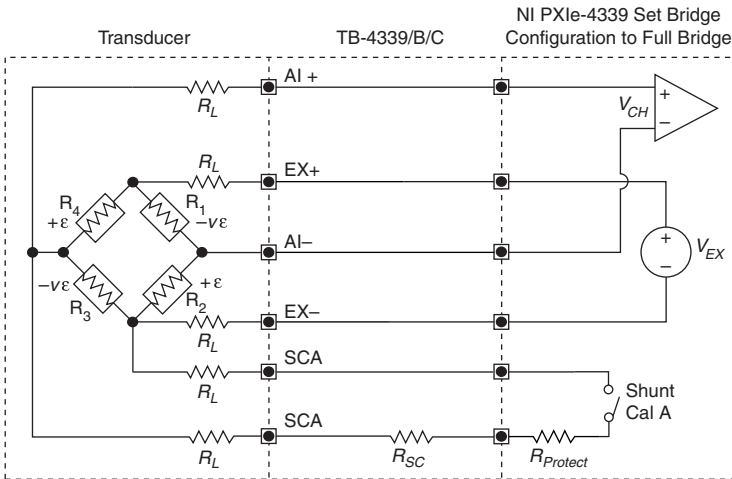
**Figure 2-15. Full-Bridge Type III Measuring Axial and Rejecting Bending Strain**



A full-bridge type III configuration has the following characteristics:

- Four active strain-gage elements. Two strain-gage elements are mounted in the direction of axial strain with one on one side of the strain specimen (top) while the other is on the opposite side (bottom). The other two act together as a Poisson gage and are mounted transverse (perpendicular) to the principal axis of strain with one on one side of the strain specimen (top) and the other on the opposite side (bottom).
- Rejects bending strain.
- Sensitivity  $\sim 1.3 \mu\text{V/V}$  per  $\mu\epsilon$ , for  $GF = 2.0$ .



**Figure 2-16.** Full-Bridge Type III Circuit Diagram

The following symbols apply to the circuit diagram and equations:

- $R_1$ —Active element measuring compressive Poisson effect ( $-v\epsilon$ ).
- $R_2$ —Active element measuring tensile strain ( $+\epsilon$ ).
- $R_3$ —Active element measuring compressive Poisson effect ( $-v\epsilon$ ).
- $R_4$ —Active element measuring the tensile strain ( $+\epsilon$ ).
- $R_L$ —Lead resistance.
- $GF$ —Gage Factor, specified by the gage manufacturer.
- $v$ —Poisson's ratio, defined as the negative ratio of transverse strain to axial strain (longitudinal) strain. Poisson's ratio is a material property of the specimen you are measuring.
- $R_{SC}$ —Shunt calibration resistor located inside the TB-4339/B/C.
- $V_{CH}$ —Measured voltage of the bridge.
- $V_{EX}$ —Excitation voltage provided by the NI PXIe-4339.
- $R_{Protect}$ —10 k $\Omega$  resistor in series with the Shunt Cal A switch to protect against external fault voltages. The total shunt cal resistance is equal to the  $R_{SC}$  and  $R_{Protect}$  series combination.
- $V_r$ —Offset compensated ratiometric bridge output defined by the following equation:

$$V_r = \left( \frac{V_{CH}(\text{strained}) - V_{CH}(\text{unstrained})}{V_{EX}} \right)$$



**Note** The ratio of the bridge output voltage and the excitation voltage is done internally on the NI PXIe-4339.

To convert module readings to strain use the following equation:

$$strain(\epsilon) = \frac{-2V_r}{GF[(v + 1) - V_r(v - 1)]}$$

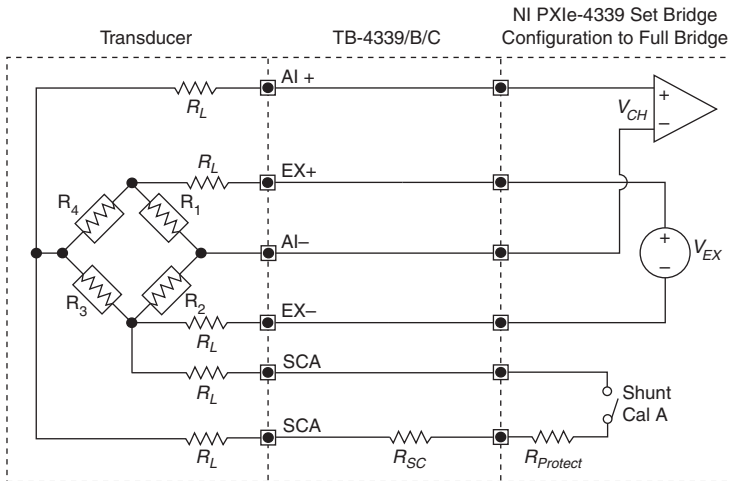
## Force, Pressure, and Torque Sensor Configurations

The NI PXIe-4339 can be used with force sensors (such as load cells), pressure sensors, or torque sensors that have the following characteristics:

- Wheatstone bridge based<sup>1</sup>
- Unamplified mV/V or V/V output<sup>2</sup>

These sensors typically use a full-bridge configuration with a 350 Ω nominal bridge resistance, but other configurations and nominal bridge resistances can be used. Figure 2-17 shows the force, pressure, torque sensor circuit diagram.

**Figure 2-17.** Force, Pressure, and Torque Sensor Circuit Diagram



The following symbols apply to the circuit diagram and equations:

- $R_1$  through  $R_4$ —Active elements of the bridge, located inside the sensor.
- $R_{SC}$ —Shunt calibration resistor located inside the TB-4339/B/C.
- $R_L$ —Lead resistance.
- $V_{CH}$ —Measured voltage (sensor output).

<sup>1</sup> Sensors that measure force, pressure, or torque through other means (for example, piezoelectric force sensors) cannot be used with the NI PXIe-4339.

<sup>2</sup> Sensors that contain a built-in voltage or current amplifier can be used with the NI PXIe-4339 in voltage mode.

- $V_{EX}$ —Excitation voltage provided by the NI PXIe-4339.
- $R_{protect}$ —10 k $\Omega$  resistor in series with the Shunt Cal A switch to protect against external fault voltages. The total shunt cal resistance is equal to the  $R_{SC}$  and  $R_{protect}$  series combination.
- $V_r$ —Offset compensated ratiometric bridge output defined by the following equation:

$$V_r = \frac{(V_{CH} \text{ (under load)} - V_{CH} \text{ (no load)})}{V_{EX}}$$



**Note** The ratio of the bridge output voltage and the excitation voltage is calculated internally on the NI PXIe-4339.

Converting module readings to physical force, pressure, or torque readings can be performed using linear, table, or polynomial scaling.

In NI-DAQmx, linear scaling for bridge-based force, pressure, and torque sensors is done based on two points which are specified as pairs of corresponding physical and electrical values: ( $electrical_1$ ,  $physical_1$ ) and ( $electrical_2$ ,  $physical_2$ ). These should be based on the calibration certificate of the sensor, if one is available; otherwise, they can be based on the specifications or data sheet of the sensor. Any two points can be used, assuming that they are far enough apart to accurately determine the slope of the linear scaling equation. For example:

- $physical_1$ —The zero point of the sensor: zero force, pressure, or torque.
- $electrical_1$ —The electrical output corresponding to the zero point of the sensor, in mV/V or V/V.
- $physical_2$ —The maximum physical reading of the sensor, or capacity: maximum load, pressure, or torque.
- $electrical_2$ —The electrical output corresponding to the maximum physical reading of the sensor, in mV/V or V/V.



**Note** Some sensor calibration certificates specify the electrical output in mV or V, not mV/V or V/V. If this is the case, divide the specified electrical output by the excitation voltage at which the calibration was performed.

The two-point linear conversion uses the following equations:

$$m = \frac{physical_1 - physical_2}{electrical_1 - electrical_2}$$

$$b = physical_1 - m \times electrical_1$$

$$physical \text{ reading} = m \times V_r + b$$

If offset nulling (bridge balancing) is used to compensate for offset, then the zero point of the sensor can be assumed to output exactly 0 V/V, simplifying these equations:

$$m = \frac{\text{physical}_2}{\text{electrical}_2}$$

$$\text{physical reading} = m \times V_r$$

When the calibration certificate of the sensor provides a table of more than two calibration points or a polynomial expression, table or polynomial scaling can produce more accurate results by compensating for non-linearity in the response of the sensor. Table scaling requires providing NI-DAQmx with a set of electrical values and corresponding physical values. Polynomial scaling requires providing NI-DAQmx with the forward and reverse coefficients of a polynomial representing the response of the sensor. If you only know one set of coefficients, you can use the DAQmx Compute Reverse Polynomial Coefficients VI/function to determine the other set. Refer to the *NI-DAQmx Help* for more information about the DAQmx Compute Reverse Polynomial Coefficients VI/function.

## Shielding and Grounding Considerations



**Caution** To ensure the specified EMC performance, operate this product only with shielded cables and accessories. Cables connected to the NI PXIe-4339 using the TB-4339/B/C terminal block must use only twisted, shielded pair cables. Use one twisted, shielded pair for each EX+/EX-, RS+/RS-, AI+/AI-, PFI0/DGND, AO+/AOGND, and T+/DGND that is cabled. Cable shields must be terminated to chassis ground at both ends.

## Module Pinout

This is the pinout represented on the front connector of the NI PXIe-4339. Refer to the [I/O Connector Signal Descriptions](#) section for definitions of each signal. Refer to the terminal block installation guide for signal locations on the terminal block.

**Table 2-1. Front Connector Signal Pin Assignments**

Front Connector Diagram			Row Number	Column A	Column B	Column C	Channel																																																																																																																																
<div style="display: flex; align-items: center;"> <div style="margin-right: 10px;"> <p>Column</p> <p>A   B   C</p> </div> <table border="1" style="border-collapse: collapse; text-align: center;"> <tr><td>32</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>31</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>30</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>29</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>28</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>27</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>26</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>25</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>24</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>23</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>22</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>21</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>20</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>19</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>18</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>17</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>16</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>15</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>14</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>13</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>12</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>11</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>10</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>9</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>8</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>7</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>6</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>5</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>4</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>3</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>2</td><td>○</td><td>○</td><td>○</td></tr> <tr><td>1</td><td>○</td><td>○</td><td>○</td></tr> </table> </div>			32	○	○	○	31	○	○	○	30	○	○	○	29	○	○	○	28	○	○	○	27	○	○	○	26	○	○	○	25	○	○	○	24	○	○	○	23	○	○	○	22	○	○	○	21	○	○	○	20	○	○	○	19	○	○	○	18	○	○	○	17	○	○	○	16	○	○	○	15	○	○	○	14	○	○	○	13	○	○	○	12	○	○	○	11	○	○	○	10	○	○	○	9	○	○	○	8	○	○	○	7	○	○	○	6	○	○	○	5	○	○	○	4	○	○	○	3	○	○	○	2	○	○	○	1	○	○	○	32	AIGND	EX+	AI+	0
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21	SCA	RS-	RS+																																																																																																																																				
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18	T5	T6	T7																																																																																																																																				
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15	AO5+	AO6+	AO7+																																																																																																																																				
14	AIGND	EX+	AI+																																																																																																																																				
13	SCA	EX-	AI-	4																																																																																																																																			
12	SCA	RS-	RS+																																																																																																																																				
11	SCA	RS-	RS+																																																																																																																																				
10	AIGND	EX+	AI+	5																																																																																																																																			
9	SCA	EX-	AI-																																																																																																																																				
8	SCA	RS-	RS+																																																																																																																																				
7	AIGND	EX+	AI+	6																																																																																																																																			
6	SCA	EX-	AI-																																																																																																																																				
5	SCA	RS-	RS+																																																																																																																																				
4	PF10	EX+	AI+	7																																																																																																																																			
3	SCA	EX-	AI-																																																																																																																																				
2	SCA	RS-	RS+																																																																																																																																				
1	RSVD	DGND	RSVD																																																																																																																																				
1	RSVD	RSVD	RSVD	No Channel																																																																																																																																			

RSVD is reserved

# I/O Connector Signal Descriptions

Table 2-2 describes the signals found on the I/O connector.

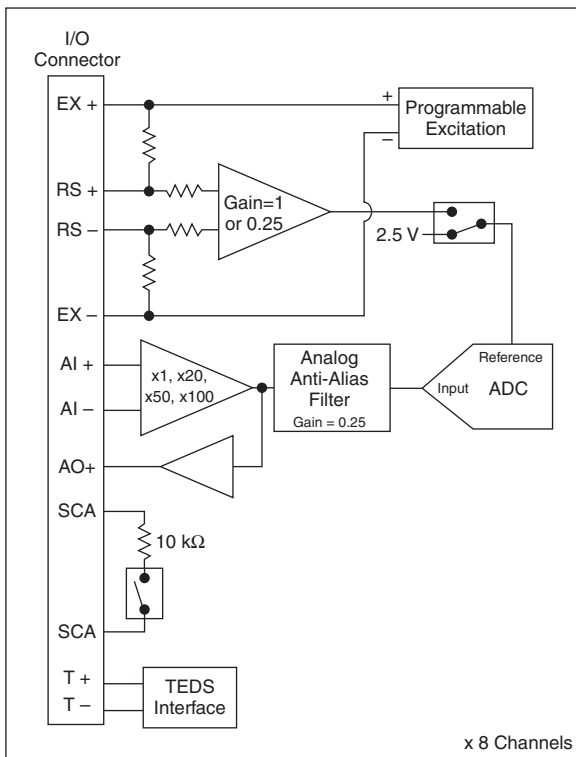
**Table 2-2.** I/O Connector Signal Descriptions

Signal Names	Direction	Description
AIGND	—	Analog Input Ground
AOGND	—	Analog Output Ground
AI<0..7>+, AI<0..7>-	Input	Analog Input Channels 0 to 7—AI+ and AI- are the positive and negative inputs of the differential analog input.
SCA<0..7>	—	These pins provide the connection point to the shunt calibration switch.
EX<0..7>+, EX<0..7>-	Output	Provides the differential bridge excitation voltage.
RS<0..7>+, RS<0..7>-	Input	Remote sense input—The remote sense pins sense the actual voltage applied to the bridge.
AO<0..7>+	Output	Wide Bandwidth Analog Output Channels 0 to 7, ground referenced to AOGND. This signal is a current-limited and external-voltage-fault protected copy of the first gain stage output.
T<0..7>+	Input/Output	TEDS sensor digital communication lines, referenced to DGND.
RSVD	—	These pins are reserved for communication with the accessory.
DGND	—	Digital ground—These pins supply the reference for module digital signals and are connected to the module digital ground.
PFIO	Input/Output	3.3 V digital signal for sending or receiving trigger and synchronization signals. This line is referenced to DGND.

# NI PXIe-4339 Block Diagram

Figure 2-18 shows the analog input circuitry block diagram of the NI PXIe-4339. The NI PXIe-4339 has two measurement modes. Voltage mode is used to measure voltages and ratiometric mode is used to provide excitation and measure from bridge-based sensors. The programmable excitation block provides the excitation voltage for bridge-based sensors. The excitation voltage level is configurable on a per channel basis. In ratiometric mode, the excitation voltage is sensed locally or remotely via the remote sense terminals (RS+ and RS-) and fed back to the ADC (Analog-to-Digital Converter) reference through a programmable gain amplifier. The gain applied when sensing the excitation voltage is automatically selected based on the selected excitation voltage level and user specified input range.

**Figure 2-18.** NI PXIe-4339 Signal Conditioning Block Diagram



The bridge output voltage is sensed through the AI+ and AI- pins and then amplified and filtered before being fed into the ADC input. The ADC then performs a ratiometric measurement of the input signal versus the reference signal to determine the actual deflection of the bridge or sensor. In voltage mode, the ADC voltage reference is fed by a stable 2.5 V voltage source.

The NI PXIe-4339 supports half-, quarter-, and full-bridge measurements. Half-bridge completion and shunt calibration switches are provided on the NI PXIe-4339. Quarter-bridge completion and shunt calibration resistors are provided on the TB-4339/B/C terminal blocks.

AO+ is a single-ended, current-limited, external-voltage-fault protected copy of the front end gain stage. Refer to the [Wide Bandwidth Analog Output](#) section for more information. Each channel also provides a transducer electronic data sheet (TEDS) interface. This interface can read the TEDS information from supported sensors to provide plug and play identification of the sensor and scaling information.

## Wide Bandwidth Analog Output

The wide bandwidth analog output voltage is a buffered version of the output of the first stage of the input signal chain. The circuit consists of a unity gain differential to single-ended stage with current limiting and external-voltage-fault protection. The current limit is nominally 3.5 mA. This circuit is always on and the gain is determined by configuration of the first stage. The output state of the wide bandwidth analog output is undefined following power up. Table 2-3 shows the nominal gain of the wide bandwidth analog output for the various input ranges of the module.

**Table 2-3.** Wide Bandwidth Analog Output Nominal Gain

Wide Bandwidth Analog Output Gain	Voltage Mode Input Range (V)	Ratio Mode Input Range (mV/V)	
		$V_{ex} > 2.5 \text{ V}$	$V_{ex} \leq 2.5 \text{ V}$
100	$\pm 0.1$	$\pm 10$	$\pm 40$
50	$\pm 0.2$	$\pm 20$	$\pm 80$
20	$\pm 0.5$	$\pm 50$	$\pm 200$
1	$\pm 10$	$\pm 1,000$	$\pm 4,000$

## Signal Acquisition Considerations

This section contains information about signal acquisition concepts, including software scaling and equations, Delta-Sigma converters, Nyquist frequency and bandwidth, timing, triggering, and synchronization.

### Software Scaling and Equations

After you have acquired the signal of interest, you can scale this measurement to the appropriate units in software. This is done automatically for you in NI-DAQmx if using certain tasks such as strain or channel types. You also can scale the measurements manually in your application using the measurement-to-strain conversion equations provided in this document for each configuration type. The NI PXIe-4339 also supports measurements for force, pressure, torque, bridge (V/V), and custom voltage with excitation.



Finally, there are voltage-to-strain conversion functions included in LabVIEW and NI-DAQmx. In LabVIEW, the conversion function, Convert Strain Gage Reading VI, is in the **Data Acquisition»Signal Conditioning** subpalette. The prototypes for the NI-DAQ functions, `Strain_Convert` and `Strain_Buf_Convert`, are in the header file `convert.h` for C/C++, and `convert.bas` for Visual Basic.

Refer to the *Measurement Fundamentals* book of the *LabVIEW Help* for more information. The strain-gage types in these sections directly correspond to bridge selections in MAX and the LabVIEW Convert Strain Gage Reading VI.

## Nyquist Frequency and Nyquist Bandwidth

Any sampling system, such as an ADC, is limited in the bandwidth of the signals it can measure. Specifically, a sampling rate of  $f_s$  can represent only signals with frequencies lower than  $f_s/2$ . This maximum frequency is known as the *Nyquist frequency*. The bandwidth from 0 Hz to the Nyquist frequency is the *Nyquist bandwidth*.

## ADC

The NI PXIe-4339 ADCs use a conversion method known as delta-sigma modulation. This approach involves oversampling the input signal and then decimating and filtering the resulting data to achieve the desired sample rate.

## Analog Input Filters

The NI PXIe-4339 uses a combination of analog and digital filtering to provide an accurate representation of in-band signals while rejecting out-of-band signals. The filters discriminate between signals based on the frequency range, or bandwidth, of the signal. The three important bands to consider are the passband, the stopband, and the alias-free bandwidth.

The NI PXIe-4339 accurately represents signals within the passband, as quantified primarily by passband flatness and phase nonlinearity. All signals that appear in the alias-free bandwidth are either unaliased signals or signals that have been filtered by at least the amount of the stopband rejection.

## Anti-Alias Filters

A digitizer or ADC might sample signals containing frequency components above the Nyquist limit. The undesirable effect of the digitizer modulating out-of-band components into the Nyquist bandwidth is aliasing. The greatest danger of aliasing is that you cannot determine whether aliasing occurred by looking at the ADC output. If an input signal contains several frequency components or harmonics, some of these components might be represented correctly while others contain aliased artifacts.

Lowpass filtering to eliminate components above the Nyquist frequency either before or during the digitization process can guarantee that the digitized data set is free of aliased components. The NI PXIe-4339 modules employ both digital and analog lowpass filters to achieve this protection.

The NI PXIe-4339 modules include an oversampled architecture and sharp digital filters<sup>1</sup> with cut-off frequencies that track the sampling rate. Thus, the filter automatically adjusts to follow the Nyquist frequency. Although the digital filter eliminates almost all out-of-band components, it is still susceptible to aliases from certain narrow frequency bands located at frequencies far above the sampling rate. These frequencies are referred to as the ADC alias holes.

In addition to the digital filtering, the NI PXIe-4339 modules feature a fixed-frequency analog filter. The analog filter removes high-frequency components in the analog signal path before they reach the ADC. This filtering addresses the possibility of high-frequency aliasing from the narrow bands that are not covered by the digital filter.

While the frequency response of the digital filter directly scales with the sample rate, the analog filter -3 dB point is fixed. The NI PXIe-4339 automatically adjusts its oversample rate to maintain a high level of alias protection regardless of the current sampling rate.

## Passband

The signals within the passband have frequency-dependent gain or attenuation. The small amount of variation in gain with respect to frequency is called the passband flatness. The digital filters of the NI PXIe-4339 adjust the frequency range of the passband to match the sample rate. Therefore, the amount of gain or attenuation at a given frequency depends on the sample rate.

## Stopband

The filter significantly attenuates all signals above the stopband frequency. The primary goal of the filter is to prevent aliasing. Therefore, the stopband frequency scales precisely with the sample rate. The stopband rejection is the minimum amount of attenuation applied by the filter to all signals with frequencies within the stopband.

## Alias-Free Bandwidth

Any signal that appears in the alias-free bandwidth of the NI PXIe-4339 is not an aliased artifact of signals at a higher frequency. The alias-free bandwidth is defined by the ability of the filter to reject frequencies above the stopband frequency, and it is equal to the sample rate minus the stopband frequency.

## Filter Group Delay

The digital filtering performed by the NI PXIe-4339 produces a delay of many samples worth of time between when an event occurs on the input signal going into the NI PXIe-4339 and when the data associated with that event is available at the output of the acquisition and filtering process. This delay is called the group delay.

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<sup>1</sup> Looser filters with degraded alias-free bandwidth are used for sample rates <25 Hz. This is done in order to reduce the large group delays associated with filtering at lower sample rates. Refer to the *NI PXIe-4339 Specifications* document for performance at lower rates.

In order to simplify the process of acquiring data from the NI PXIe-4339 modules and correlating that data with data from other modules, the NI PXIe-4339 compensates for this group delay in the following ways:

- The Sample Clock output from the NI PXIe-4339 is generated at the point in time when the input signal is valid at the ADC input pins. When acquiring data, the NI PXIe-4339 generates a Sample Clock, then waits for the data associated with that Sample Clock to be acquired, then returns that data. As a result, any other acquisitions timed with this Sample Clock line up with the data returned by the NI PXIe-4339.
- Any triggers generated or received by the NI PXIe-4339 are interpreted based on their relationship to the Sample Clock being generated. For example, a Start Trigger that starts an acquisition results in data from the next Sample Clock being returned as the first point in the acquisition. Refer to the [Triggering and Filter Delay](#) section for more details about how this affects analog trigger events.
- On demand software sampling returns a single sample from an acquisition running at the maximum supported sample rate of the module. For any on-demand, software timed acquisition, the NI PXIe-4339 waits for the group delay to elapse before returning the sample. As a result, the data returned aligns closely in time with when the data was requested and is delayed by the sum of the analog input delay and digital filter delay.<sup>1</sup>
- The maximum sample rate of the NI PXIe-4339 is 25.6 kS/s.

## Supported Data Rates

The NI PXIe-4339 supports rates of 1 S/s to 25.6 kS/s.

## Hardware-Timed Single Point Acquisitions

Hardware-Timed Single Point (HWTSP) is a hardware timed acquisitions mode in which a digital hardware signal (SampleClock) controls the rate of the acquisition and data that is transferred to a PXI Express controller or computer through HWTSP operations. The SampleClock signal can be imported or internally generated in the NI PXIe-4339 using the sample rate configured in the NI-DAQmx task.

When transferring data to the PXI Express controller or computer, HWTSP operations are used to read single samples at known time intervals. While buffered operations are optimized for high throughput, HWTSP operations are optimized for low latency. These features make HWTSP ideal for real-time control applications. HWTSP operations, in conjunction with the wait for next sample clock function, provide more deterministic synchronization between the software layer and the hardware layer. Refer to the *NI-DAQmx Hardware-Timed Single Point Lateness*

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<sup>1</sup> The maximum sample rate of the NI PXIe-4339 is 25.6 kS/s. In addition to the fixed analog input delay, you must also account for the digital-filter group delay. For 25.6 kS/s, the digital filter group delay is

$$1.90976 \text{ ms} + \frac{48.5 \text{ S}}{25600 \text{ S/s}} = 3.8043 \text{ ms}$$

If a 10 V range is used, total delay is 3.8043 ms + 6.1 μs = 3.8104 ms. Refer to the *NI PXIe-4339 Specifications* for more information.

Checking document for more information. To access this document, go to [ni.com/info](http://ni.com/info) and enter the Info Code `daqhwtsp`.

## Hardware-Timed Single Point Acquisition Model

The HWTSP data path is optimized for low-latency applications and is different than that which is used in buffered acquisition model (default).

When in HWTSP mode, the filtering and sampling systems can be modeled as being decoupled, which allows you to configure the filter and sampling rate independently.

Figure 2-19 shows the HWTSP data path model.

**Figure 2-19. HWTSP Data Path Model**



The ADC samples the input stream and returns it to the PXI Express controller or computer at every SampleClock signal.

## Maximum HWTSP Rate Analysis

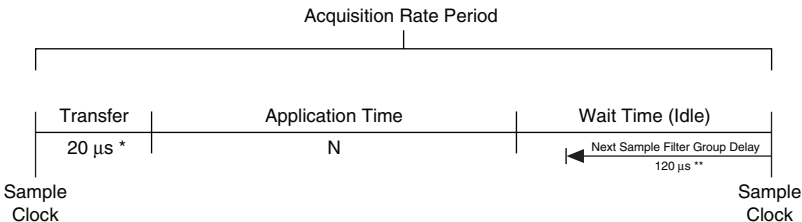
When in HWTSP, the maximum achievable acquisition rate, without missing a sample, is affected by both the transfer and application time. Refer to Figure 2-20.

$$Rate_{Max} = \frac{1}{Transfer\ Time + Application\ Time}$$



**Note** HWTSP can notify software if it cannot keep up with the acquisition rate. Refer to the *Hardware-Timed Single Point Sample Mode* topic in the *NI-DAQmx Help* for more information.

**Figure 2-20. Transfer Time and Application Time Relationship**



\*Transfer time may vary depending on system.

\*\*120 μs is the approximate group delay of the 2 kHz filter for input frequencies < 1 kHz (passband of the filter).



**Note** For control applications, it is important to consider the group delay of the data being acquired and analyzed when calculating the control system bandwidth. Regardless of the sample rate, the bandwidth of the system is as follows:

$$\text{bandwidth} = \frac{1}{\text{Transfer Time} + \text{Application Time} + \text{Group Delay}}$$

## 2 kHz Control Loop Rate Calculation Example

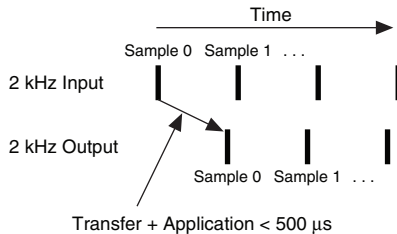
Figure 2-21 represents a typical control system in which you have a process to control, a DAQ device to do the acquisitions and generate stimulus, and a PXI Express controller or computer to do the data processing and determine the proper AO value and returning it to the process.

**Figure 2-21.** Typical Control System



To successfully close a 2 kHz control loop, make sure that the time between the time the AI sample is acquired and the time the AO stimulus is generated is <500 μs. Refer to Figure 2-22.

**Figure 2-22.** Input and Output of a Control System with Bandwidth ≥2 kHz



To make sure that your application can run and control a process at 2 kHz, and that the first output is generated within the first sample period, make sure that the following conditions are satisfied:

$$500 \mu\text{s} \leq \text{Transfer Time} + \text{Application Time} \tag{2-1}$$

Where:

*Transfer Time*—the time it takes to transfer samples between the DAQ device and the PXI Express controller or computer.

*Application Time*—the time it takes for the PXI Express controller or computer to analyze the acquired data and generate the AO stimulus.

Using Equation 2-1 and the Transfer Time from the sample system described in this section, you can determine that an application time of 480 μs is required to close a 2 kHz control loop.

$$\text{Application Time} \leq 500 \mu\text{s} - \text{Transfer Time}$$

$$\text{Application Time} \leq 500 \mu\text{s} - 20 \mu\text{s}$$

$$\text{Application Time} \leq 480 \mu\text{s}$$

Any application taking more than 480  $\mu\text{s}$  will fail to close the 2 kHz control loop.

When analyzing the bandwidth of the system, you must consider the group delay of all the components of the system. When using only the NI PXIe-4339 internal 2 kHz filter, the bandwidth of the control loop is as follows:

$$\text{Control Bandwidth} = \frac{1}{\text{Transfer Time} + \text{Application Time} + \text{Filter Group Delay}}$$

$$\text{Control Bandwidth} = \frac{1}{20 \mu\text{s} + 480 \mu\text{s} + 120 \mu\text{s}}$$

$$\text{Control Bandwidth} = 1613 \text{ kHz}$$



**Note** You can increase the bandwidth of the system by either reducing the application time or by using another filter option with lower group delay.

## Timing and Triggering

This section contains information about timing and triggering theory of operation.

### Sample Clock Timebase

The ADCs require an oversample clock to drive the conversion. The oversample clock frequency is greater than the sample rate. On the NI PXIe-4339 modules the oversample clock is produced from a 100 MHz reference clock. This 100 MHz reference clock can be supplied either by an onboard oscillator or by the PXI Express backplane 100 MHz clock. Multiple modules can be synchronized by selecting the PXI Express backplane 100 MHz clock as the reference clock source for all the modules. Refer to the [Reference Clock Synchronization](#) section for more information.

### External Clock

The NI PXIe-4339 ADCs cannot be clocked from external sources such as encoders or tachometers. However, signal processing features in the Sound and Vibration Measurement Suite often provide an excellent alternative to external clocking in encoder and tachometer applications. Visit [ni.com/soundandvibration](http://ni.com/soundandvibration) for more information about the Sound and Vibration Measurement Suite.

### Digital Triggering

You can configure the NI PXIe-4339 modules to start an acquisition in response to a digital trigger signal from one of the PXI Express backplane trigger lines or the PFI from the front connector. The trigger circuit can respond either to a rising or a falling edge.

## Analog Triggering

Analog triggering allows you to trigger your application based on an input signal and trigger level you define. You can configure the analog trigger circuitry to monitor any input channel acquiring data. Choosing an input channel as the trigger channel does not change the input channel acquisition specifications.

The analog trigger signal can be used as a reference trigger only. In a reference-triggered acquisition, you configure the module to acquire a certain number of pre-trigger samples and a certain number of post-trigger samples. Reference-triggered acquisitions can therefore only be configured as Finite tasks. The analog trigger on the NI PXIe-4339 cannot be used as a start trigger. This restriction is a result of the way the module compensates for the filter group delay.

When using an analog reference trigger, the module first waits for the specified number of pre-trigger samples to be acquired. Once enough pre-trigger samples are acquired, the reference trigger will occur the next time the analog trigger condition is met. You also can route the resulting reference trigger event to supported digital terminals. Refer to the device panels in MAX for additional information.

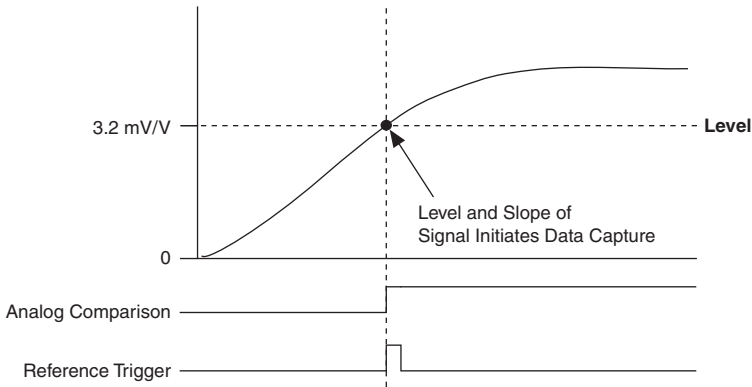
During repetitive triggering on a waveform, you might observe jitter because of the uncertainty of where a trigger level falls compared to the actual digitized data. Although this trigger jitter is never greater than one sample period, it might be significant when the sample rate is only twice the bandwidth of interest. This jitter usually has no effect on data processing, and you can decrease this jitter by sampling at a higher rate.

You can use several analog triggering modes with the NI PXIe-4339 modules, for instance analog edge, analog edge with hysteresis, and window triggering.

## Analog Edge Triggering

For analog edge triggering, configure the module to detect a certain signal level and slope, either rising or falling. Figure 2-23 shows an example of rising edge analog triggering. The analog comparison becomes true when the signal starts below Level and then crosses above Level.

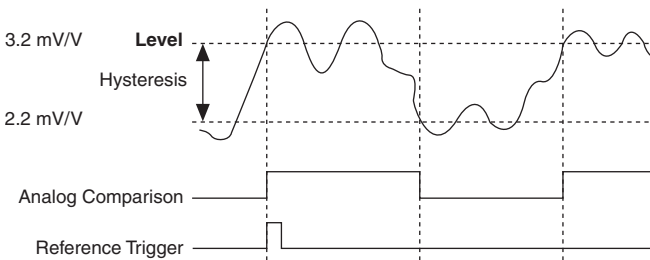
**Figure 2-23.** Analog Level Trigger on Rising Slope



## Analog Edge Triggering With Hysteresis

When you add hysteresis to analog edge triggering, you add a window above or below the trigger level. This triggering mode often is used to reduce false triggering due to noise or jitter in the signal. For example, if you add a hysteresis of 1 mV/V to the example in Figure 2-23, which uses a level of 3.2 mV/V, the signal must start at or drop below 2.2 mV/V to arm the trigger. The analog comparison becomes true when the signal rises above 3.2 mV/V and becomes false when it falls below 2.2 mV/V, as shown in Figure 2-24.

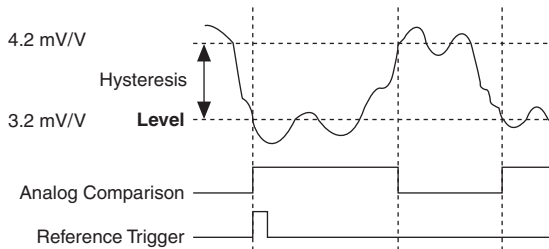
**Figure 2-24.** Analog Edge Triggering with Hysteresis on Rising Slope





When using hysteresis with a falling slope, the trigger is armed when the signal starts above Level plus the hysteresis value and asserts when the signal crosses below Level. For example, if you add a hysteresis of 1 mV/V to a level of 3.2 mV/V, the signal must start at or rise above 4.2 mV/V to arm the trigger. The analog comparison becomes true as the signal falls below 3.2 mV/V and becomes false when it rises above 4.2 mV/V, as shown in Figure 2-25.

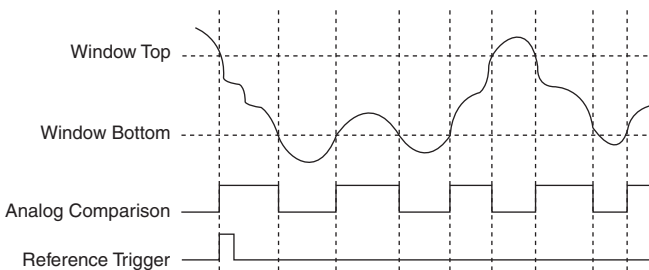
**Figure 2-25. Analog Edge Triggering with Hysteresis on Falling Slope**



## Window Triggering

A window trigger occurs when an analog signal either passes into (enters) or passes out of (leaves) a window defined by two levels. Specify the levels by setting a value for the top and bottom window boundaries. Figure 2-26 demonstrates a trigger that acquires data when the signal enters the window. You can also program the trigger circuit to acquire data when the signal leaves the window.

**Figure 2-26. Window Triggering**



## Triggering and Filter Delay

The NI PXIe-4339 can use a digital trigger signal from the backplane or the PFI from the front connector as either a start trigger initiating an acquisition, or a reference trigger in the middle of an acquisition. The NI PXIe-4339 can also generate an analog trigger event from its digitized ADC data. As a result of the way the NI PXIe-4339 modules adjust for its digital filter group delay, analog triggers can only act as reference triggers.

In all cases, the NI PXIe-4339 interprets triggers based on where they occur in time. The hardware automatically compensates for its group delay such that data from this module will line up closely in time with the occurrence of the trigger event. However, the group delay affects how

long it takes to receive data when starting an acquisition. Since linear phase FIR filters are used in the digital filtering, it is necessary to wait for the filter group delay to elapse after sending a sync pulse before the start trigger can be correctly handled in time. Step 6 in the [Reference Clock Synchronization](#) section allows NI-DAQmx to handle this delay automatically. After the digital start trigger, you cannot read data for the first sample in software until the digital filter group delay has elapsed. Therefore, it takes a total of twice the digital filter group delay to start an acquisition. You can insert additional time between when the sync pulse occurs and when the start trigger occurs. This will not affect the time it takes before samples are available after the start trigger, which is always the group delay time. Group delay time increases as sample rates decrease. Refer to the *NI PXIe-4339 Specifications* document for details regarding the group delay at different sample rate.

## Synchronization

Some applications require tight synchronization between input and output operations on multiple modules. Synchronization is important to minimize skew between channels or to eliminate clock drift between modules in long-duration operations. You can synchronize the analog input operations on two or more NI PXIe-4339 modules to extend the channel count for your measurements. In addition, the NI PXIe-4339 can synchronize with certain DSA modules, such as the NI PXIe-449x modules, using Reference Clock Synchronization.

## Reference Clock Synchronization

With reference clock synchronization, master and slave modules generate their ADC oversample clock from the shared 100 MHz reference clock from the PXI Express backplane (PXIe\_CLK100). The backplane supplies an identical copy of this clock to each peripheral slot. In addition, multiple chassis can be synchronized by using a timing and synchronization board to lock the 100 MHz clock across chassis.

When you acquire data from multiple modules within the same NI-DAQmx task, NI-DAQmx will automatically handle all of the Reference Clock Synchronization details required to synchronize the modules within the task. This is known as a Multi-Device Task.

To perform Reference Clock Synchronization when using multiple NI-DAQmx tasks that are acquiring at the same rate, complete the following steps to synchronize the hardware.

1. Specify PXIe\_CLK100 as the reference clock source for all modules to force all the modules to lock to the reference clock on the PXI Express chassis.
2. Choose an arbitrary NI PXIe-4339 master module to issue a sync pulse on one of the PXI Express Trigger lines. The sync pulse resets the ADCs and oversample clocks, phase aligning all the clocks in the system to within nanoseconds.
3. Configure the rest of the modules in your system to receive their sync pulse from the sync pulse master module. This will ensure all ADCs are running in lockstep.
4. Choose one module to be the start trigger master. This does not have to be the same module you chose in step 3.

5. Configure the rest of the modules in your system to receive their start trigger from the start trigger master module. This ensures that all modules will begin returning data on the same sample.
6. Set the synchronization type of the Start Trigger slaves at **DAQmx Trigger»Advanced»Synchronization»Synchronization Type** to Slave and that of the Master to Master.
7. Query **DAQmx Timing»More»Synchronization Pulse»Synchronization Time** on all modules being synchronized, choose the maximum value and set that as the **DAQmx Timing»More»Synchronization Pulse»Minimum Delay To Start** on the module from which the synchronization pulse originates.
8. Commit all of the sync pulse slave module tasks using the DAQmxTaskControl VI/Function. This sets them up to expect the sync pulse from the master.
9. Commit the sync pulse master module task using the DAQmxTaskControl VI/Function. This will issue the sync pulse.
10. Start all of the start trigger slave module tasks. This sets them up to expect the start trigger from the master.
11. Start the start trigger master module task. You can now acquire data.



**Tip** Consider using a Multi-Device task when synchronizing multiple devices at the same rate.



**Tip** You can find example VIs in the NI Example Finder. Select **Help»Find Examples** to launch the NI Example Finder.

Consider the following caveat to using Reference Clock synchronization:

- The NI PXIe-4339 automatically compensates for its filter group delay. However, some other device families do not compensate for their filter delay. In this case, manually compensate for group delay in the waveforms when you synchronize between device families if this level of synchronization is required for your application.

## TEDS

The NI PXIe-4339 supports communicating with Transducer Electronic Data Sheet (TEDS)-enabled sensors (IEEE 1451.4 Class 2). TEDS-enabled sensors carry a built-in, self-identification EEPROM containing a table of parameters and sensor information. This allows your data acquisition system to automatically detect and configure the sensors.

TEDS contains information about the sensor such as calibration, sensitivity, and manufacturer information. This information is accessible in Measurement & Automation Explorer (MAX), VIs in LabVIEW, or by calling the equivalent function calls in a text-based ADE.

For more information about TEDS plug and play sensors, refer to [ni.com/pnp](http://ni.com/pnp).

## Configuring and Using TEDS in Software

To manually configure TEDS in MAX, right-click the NI PXIe-4339 module within the Configuration tree. Then select **Configure TEDS** from the pop-up menu.

To programmatically configure TEDS, call the DAQmx Configure TEDS VI.

## Accessory Auto-Detection

SC Express modules automatically detect compatible accessories or terminal blocks. The RSVD pins on the I/O connector provide power to the accessories as well as digital communication lines. This allows software to detect when accessories are inserted or removed. In addition, software can automatically identify the specific terminal block as well as access any calibration or scaling information associated with the terminal block.

MAX allows you to see what accessories are currently connected to your module. In MAX, expand **Devices and Interfaces** and locate your module. If a terminal block is connected to your module, it will be displayed beneath the module. Unsupported terminal blocks appear in MAX with an X next to them.

NI-DAQmx property nodes can be used to programmatically access information about connected accessories in your application. Refer to the *NI-DAQmx Help* for documentation about programmatically accessing accessory status.

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# SC Express Considerations

This chapter details the clock and trigger functionality available through the PXI Express chassis.

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## SC Express Clock and Trigger Signals

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### PXIe\_CLK100

PXIe\_CLK100 is a common, low-skew 100 MHz reference clock used for synchronization of multiple modules in a PXI Express measurement or control system. The PXI Express backplane is responsible for generating PXIe\_CLK100 independently to each peripheral slot in a PXI Express chassis. For more information, refer to the *PXI Express Specification* at [www.pxisa.org](http://www.pxisa.org).

### PXIe\_SYNC100

PXIe\_SYNC100 is a common, low-skew 10 MHz reference clock with a 10% duty cycle for synchronization of multiple modules in a PXI Express measurement or control system. The PXI Express backplane is responsible for generating PXIe\_SYNC100 independently to each peripheral slot in a PXI Express chassis. PXIe\_SYNC100 allows modules using PXIe\_CLK100 as their reference to recreate the timing of the PXI\_CLK10 signal while taking advantage of the lower skew of PXIe\_CLK100. For more information, refer to the *PXI Express Specification* at [www.pxisa.org](http://www.pxisa.org).

### PXI\_CLK10

PXI\_CLK10 is a common, low-skew 10 MHz reference clock for synchronization of multiple modules in a PXI measurement or control system. The PXI backplane is responsible for generating PXI\_CLK10 independently to each peripheral slot in a PXI chassis. In PXI Express chassis, the PXI\_CLK10 signal is in phase with PXIe\_CLK100.



**Note** PXI\_CLK10 cannot be used as a reference clock for SC Express modules.

### PXI Triggers

A PXI/PXI Express chassis provides eight bused trigger lines to each module in a system. Triggers may be passed from one module to another, allowing precisely timed responses to asynchronous external events that are being monitored or controlled. Triggers can be used to synchronize the operation of several different PXI peripheral modules.

In a PXI chassis with more than eight slots, the PXI trigger lines may be divided into multiple independent buses. Refer to the documentation for your chassis for details.

## PXI\_STAR Trigger

In a PXI Express system, the Star Trigger bus implements a dedicated trigger line between the system timing slot and the other peripheral slots. The Star Trigger can be used to synchronize multiple modules or to share a common trigger signal among modules.

A system timing controller can be installed in the system timing slot to provide trigger signals to other peripheral modules. Systems that do not require this functionality can install any standard peripheral module in this system timing slot.

An SC Express module receives the Star Trigger signal (PXI\_STAR) from a System timing controller. PXI\_STAR can be used as a trigger signal for input operations.

An SC Express module is not a System timing controller. An SC Express module can be used in the system timing slot of a PXI system, but the system will not be able to use the Star Trigger feature.

## PXIe\_DSTAR<A..C>

PXI Express devices can provide high-quality and high-frequency point-to-point connections between each slot and a system timing slot. These connections come in the form of three low-voltage differential star triggers that route between a PXI Express system timing controller and a peripheral device. Using multiple connections simplifies the creation of applications because of the increased routing capabilities.

Table 3-1 describes the three differential star (DSTAR) lines and how they are used.

**Table 3-1. PXIe\_DSTAR Line Descriptions**

Trigger Line	Purpose
PXIe_DSTARA	Distributes high-speed, high-quality clock signals from the system timing slot to the peripherals (input).
PXIe_DSTARB	Distributes high-speed, high-quality trigger signals from the system timing slot to the peripherals (input).
PXIe_DSTARC	Sends high-speed, high-quality trigger or clock signals from the peripherals to the system timing slot (output).

The DSTAR lines are only available for PXI Express devices when used with a PXI Express system timing module. For more information, refer to the *PXI Express Specification* at [www.pxisa.org](http://www.pxisa.org).

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# Offset Nulling (Bridge Balancing)

When you install a bridge-based sensor, the bridge probably will not output exactly 0 V when not under load. Slight variations in resistance among the bridge legs generate some nonzero initial offset voltage. Use the DAQmx Perform Bridge Offset Nulling Calibration VI/function or the DAQ Assistant to perform an offset nulling calibration, which will apply software compensation for the bridge.

NI-DAQmx will measure the bridge while not under load, and then use this measurement as the initial bridge voltage when scaling readings from the bridge. This method is simple, fast, and requires no manual adjustments. The disadvantage of the software compensation method (in contrast to hardware compensation) is that software compensation does not physically remove the offset of the bridge. If the offset is large enough, it limits the amplifier gain you can apply to the output voltage, thus limiting the dynamic range of the measurement. The NI PXIe-4339 does not have any internal hardware nulling circuitry, however, its input range is sufficiently wide so that the inputs will not saturate even with a relatively large initial bridge offset.

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