
PXIe-4468 Calibration procedure

September 2022

PXIe-4468 Calibration Procedure

This document contains the verification and adjustment procedures for the PXIe-4468 with either BNC or mini-XLR connectors. Use the procedures in this document to automate calibration or to conduct manual calibration. Review and become familiar with the entire procedure before beginning the calibration process.

Contents

Terms and Definitions	3
Calibration Overview.....	4
Calibration Condition Guidelines	5
Calibration Resources	5
Required Software.....	5
Recommended Documentation	6
Test Equipment	6
Warm Up the DUT	8
Perform Self-Calibration	8
Perform Verification	9
AI Offset Accuracy Verification.....	9
AI Gain Accuracy Verification	12
AI Gain Flatness Verification	14
IEPE Current Verification.....	17
AO Differential Offset Accuracy Verification.....	19
AO Differential Gain Accuracy Verification.....	22
AO Gain Flatness Verification.....	26
AO Common-Mode Gain and Offset Verification	29
Timebase Frequency Accuracy Verification	31
Perform Adjustment.....	34
AI/AO Gain and Offset Adjustment	34
Timebase Adjustment	35
Perform Reverification	36
Update the Onboard Calibration Information.....	37
Revision History.....	37
NI Services	38

Terms and Definitions

DUT	DUT is an acronym for Device Under Test and refers to the NI product being calibrated. For this procedure, DUT refers to the PXIe-4468.
As-Found Limits	These limits are derived from the published specifications for the DUT. NI uses these limits to determine if the DUT is performing within the recommended calibration interval specifications at the time of calibration and before any adjustment is performed.
As-Left Limits	These limits are derived from the published specifications for the DUT minus guardband to ensure a high probability that the DUT will meet its specifications over the next recommended calibration interval.
Functional Test	Functional Tests determine whether the DUT is operating correctly. Functional tests are not directly related to performance specifications.
Verification	Verification evaluates the measured calibration results against the defined As-Found Limits. The result of the evaluation is expressed as a Pass/Fail condition in the calibration certificate using an established evaluation formula.
Adjustment	Adjustment performs a set of operations on the DUT to optimize the measurement performance and conform it to the assigned calibrated values.
Reverification	Reverification evaluates the measured calibration results against the As-Left limits after adjustment. The As-Left limits may be tighter than the As-Found limits.
Recommended Calibration Interval	This interval indicates the recommended period between each round of verification and adjustment of the DUT. There is a high probability that, within this interval, the DUT will remain within the published warranted performance specifications. Some measurement DUTs have warranted specifications for different calibration intervals, for example: 24 hours, 90 days, 1 year, and 2 years. In this case, the specification depends on the calibration cycle chosen by the user.

Calibration Overview

Recommended Calibration Interval

2 years

Password

NI



Note

This is the default password for all password-protected operations. This password is site-specific.

Task	Estimated Test Time	Operator Connections	Test Points
Setup	10 minutes	—	—
Warm Up	15 minutes	—	—
Verify, Adjust, and Reverify	19 minutes	36	344
Verify Only	8 minutes	17	171
Adjust Only	3 minutes	2	2



Note

Estimated test times assume the user is conducting a manual calibration. For most procedures, automating the calibration significantly reduces test times.

Environmental Conditions	Verification	Adjustment
Ambient temperature	23 °C ± 5 °C	23 °C ± 5 °C
Internal DUT temperature range	Tcal ± 5 °C	Tcal ± 5 °C
Relative humidity	Between 20% and 80%, noncondensing	

Calibration Condition Guidelines

- Keep cabling as short as possible. Long cables act as antennas, picking up extra noise that can affect measurements.
- Ensure that all connections to the DUT are secure.
- Allow adequate warm up time for all components of the calibration system.
- Make all connections as shown in diagrams.
- Use shielded copper wire for all cable connections to the DUT.
- Use twisted-pair wires to eliminate noise and thermal offsets.
- Ensure that the PXI/PXI Express chassis fan speed is set to HIGH, that the fan filters are clean, and that the empty slots contain filler panels. For more information, refer to the Maintain Forced-Air Cooling Note to Users document available at ni.com/manuals.
- If a DUT fails reverification after adjustment, ensure that the Test Conditions have been met before returning the DUT to NI.
- If the coupling changes from DC to AC (for example, on the first gain verification point tested), commit the configuration using the DAQmx Control Task VI and wait 5 seconds for the input to settle. Subsequent gain verification points, which do not change the coupling, do not require a delay.

Calibration Resources

Required Software

**Note**

Ensure that the most recent version of the required driver software is installed before conducting the calibration.

Install the following software on the calibration system:

- DAQmx

Recommended Documentation

Go to ni.com/docs to locate the following documentation for more information when performing this calibration:

- PXIe-4468 Getting Started Guide
- PXIe-4468 Specifications
- NI-DAQmx Readme
- NI-DAQmx Help
- LabVIEW Help
- NI-DAQmx C Reference Help
- NI-DAQmx .NET Help Support for Visual Studio

Test Equipment

This section details the equipment NI recommends for each test performed as part of this calibration procedure.



NI Calibration Executive Users

Refer to the Calibration Executive Help to find an updated list of test equipment for this calibration procedure.

Standard	Recommended Model	Where Used	Functional Requirement(s)
Calibrator	Fluke 5730A	AI Gain AI Flatness	Frequency Range: 40 Hz to 100 kHz Voltage Range: up to 6.3 V _{rms}
Digital Multimeter (DMM)	Keysight (Agilent) 3458A	AO Differential Offset AO Differential Offset and Gain Adjustment	DC Voltage Input Range: 100mV, 1 V, 10 V
		AO Differential Gain AO Differential Flatness	AC Voltage Input Range: 1 V _{rms} , 10 V _{rms} Frequency Range: 20Hz to 100 kHz
Function Generator	Keysight (Agilent) 33250A series	Timebase Frequency	Frequency Range: up to 90 kHz
PXI Express Chassis	NI PXIe-1082 NI PXIe-1085 NI PXIe-1075 NI PXIe-1065 NI PXIe-1062Q	All Tests	
System Controller	NI PXIe-8135	All Tests	A PXI Express controller or MXI Express Card
mXLR (F) to BNC (M) Cable (quantity 1)	NI 140150-0R46	All Tests (mXLR Variant)	Length: ≤ 0.5m
BNC (M) to BNC (M) Cable (quantity 1)	Pomona Electronics 5697	All Tests (BNC Variant)	Length: ≤ 0.5m
BNC (F) to Banana Adapter (quantity 1)	Pomona Electronics 1269	AI Gain AI Flatness AO Offset AO Gain AO Flatness AO Offset and Gain Adjustment	

Banana to Banana Cable (quantity 1)	Pomona Electronics B-4-2	AO Differential Gain and Offset	Length: ≤ 0.5m
Banana to Alligator Clip Cable (quantity 2)	Pomona Electronics 1166-12-0 (Black) 1166-12-2 (Red)	AO Differential Gain and Offset	Length: ≤ 0.5m

Warm Up the DUT

Warm up time starts after the installed DUT is powered on in the chassis. Warm up time resets after the DUT is removed from the chassis. This DUT requires 15 minutes to warm up prior to conducting any tests.



Note

Observe adequate Warm up time for all components of the calibration system.

Perform Self-Calibration

Self-calibration should be performed after the DUT has warmed up for the recommended time period. This function measures the onboard reference voltage of the DUT and adjusts the self-calibration constants to account for any errors caused by short-term fluctuations in the environment.

Complete the following steps to conduct self-calibration using Measurement & Automation Explorer (MAX).



Note

Disconnect all external signals before beginning self-calibration.

1. Launch MAX.
2. Select My System»Devices and Interfaces»NI PXIe-4468.
3. Start self-calibration using one of the following methods:
4. Click **Self-Calibrate** in the upper right corner of MAX.

- Right-click the name of the DUT in the MAX configuration tree and select **Self-Calibrate** from the drop-down menu.

Perform Verification

AI Offset Accuracy Verification

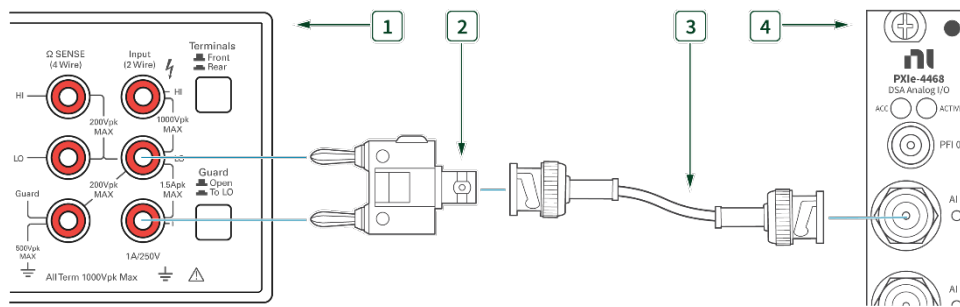
Test Limits

Table 1: AI Offset Verification Limits

	Device Gain (dB)	As-Found Test Limit		As-Left Test Limit	
		Lower Limit (mV)	Upper Limit (mV)	Lower Limit (mV)	Upper Limit (mV)
DC Coupled	-20	-5.0	5.0	-0.9	0.9
	-10	-2.0	2.0	-0.3	0.3
	0	-0.5	0.5	-0.1	0.1
	10	-0.2	0.2	-0.05	0.05
	20	-0.1	0.1	-0.04	0.04
	30	-0.1	0.1	-0.04	0.04

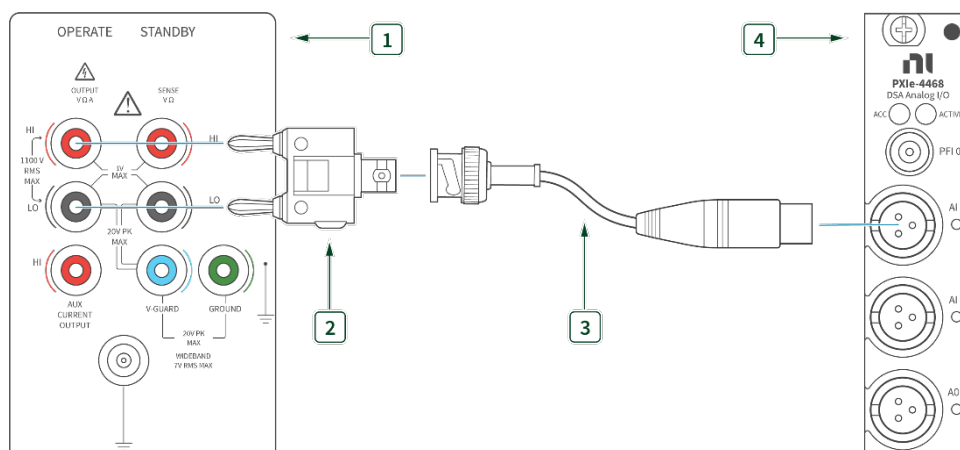
Initial Test Connection

Figure 1. Initial Connection for AI Offset-BNC



- | | |
|-------------------------|-----------------------|
| 1. Calibrator | 3. BNC – BNC Cable |
| 2. Banana – BNC Adapter | 4. PXIe-4468 with BNC |

Figure 2. Initial Connection for AI Offset-mXLR



- | | |
|-------------------------|------------------------|
| 1. Calibrator | 3. BNC – mXLR Cable |
| 2. Banana – BNC Adapter | 4. PXIe-4468 with mXLR |

Verification Procedure

Complete the following procedure to verify the AI offset accuracy.

Repeat 2 times, once for each channel.

1. Connect the AI channel under test to the Calibrator as shown in **Figure 1** or **Figure 2**.

- Configure the calibrator to output 0V DC, with GND engaged.

Repeat 6 times, once for each gain setting.

- Create and configure an AI voltage task on the DUT as shown in **Table 2**.

Table 2: AI Offset Verification Configuration

Configuration	Value
Physical channels	<i>Dev_name/aix</i>
Gain*	Gain from Table 1
Coupling	DC
Terminal configuration	Pseudodifferential
Excitation (IEPE)	0 (A)
Acquisition mode	Finite number of samples
Rate	250000
Samples per channel	125000

* As you configure the AI voltage task, refer to **Table 3** for the maximum and minimum voltages to specify when creating the task to ensure the specified gain range is used on the module. The module automatically selects the gain range based on the maximum and minimum voltages you supply when you create the task.

Table 3: Gain Range and Corresponding Max and Min Voltages

Desired Gain Range (dB)	Max Voltage (V)	Min Voltage (V)
-20	42.4	-42.4
-10	31.6	-31.6
0	10.0	-10.0
10	3.16	-3.16
20	1.00	-1.00

30

0.316

-0.316

4. Start the task.
5. Acquire readings with the DUT.
6. On a per channel basis, average all of the acquired samples.
7. Stop and clear the task.
8. Compare the averaged values to the appropriate limits in **Table 1**. The average is the offset at the tested gain setting.

AI Gain Accuracy Verification

Test Limits

Table 4: AI Gain Verification Limits

Device Gain (dB)	Calibrator Output		As-Found Test Limit		As-Left Test Limit	
	Amplitude (V_{rms})	Frequency (Hz)	Lower Limit (V_{rms})	Upper Limit (V_{rms})	Lower Limit (V_{rms})	Upper Limit (V_{rms})
-20	6.3	1000	6.28189	6.31816	6.28551	6.31452
-10	6.3	1000	6.28189	6.31816	6.28551	6.31452
0	6.3	1000	6.28189	6.31816	6.29637	6.30363
10	2.0	1000	1.99425	2.00576	1.99885	2.00115
20	0.63	1000	0.62819	0.63182	0.62964	0.63036
30	0.2	1000	0.19943	0.20058	0.19988	0.20012

Initial Test Connection



Note

Initial test connection is same as AI Offset, as shown in **Figure 1** or **Figure 2**.

Verification Procedure

Complete the following procedure to verify the AI gain accuracy.

Repeat 2 times, once for each channel.

1. Connect the AI channel under test to the Calibrator as shown in **Figure 1** or **Figure 2**.

Repeat 6 times, once for each gain setting.

2. Configure the calibrator to generate an output with the amplitude and frequency from **Table 4**.
3. Create and configure an AI Voltage channel task using the values in **Table 5**.

Table 5: AI Gain Verification Configuration

Configuration	Value
Physical Channels	<i>Dev_name/aix</i>
Gain*	Gain from Table 4
Coupling	AC
Terminal Configuration	Pseudodifferential
Excitation (IEPE)	0 (A)
Acquisition mode	Finite number of samples

Rate	250000
Samples per channel	125000

*Refer to **Table 3** for the maximum and minimum voltages to specify to ensure the specified gain range is used on the module.

4. Start the task.
5. Acquire readings with the DUT.
6. Calculate the RMS amplitude of the acquired fundamental harmonic. Compare this amplitude to the appropriate voltage limits in **Table 4**. The calculated amplitude is used to verify the gain accuracy of the channel under test at the tested gain setting.

As an example, use the Extract Single Tone Information VI to help calculate RMS. Note that the output of this VI is peak amplitude, and must be divided by $\sqrt{2}$ to convert to RMS.

7. Stop and clear the task.

AI Gain Flatness Verification

Test Limits

Table 6: AI Flatness Verification Limits

Device Gain (dB)	Calibrator Output Frequency (kHz)	As-Found Test Limit	
		Lower Limit	Upper Limit
-10 and -20	1	$V_{1\text{kHz}}$	
	20	$0.97724 * V_{1\text{kHz}}$	$1.02329 * V_{1\text{kHz}}$
	45	$0.93325 * V_{1\text{kHz}}$	$1.07152 * V_{1\text{kHz}}$
	100	$0.89125 * V_{1\text{kHz}}$	$1.12202 * V_{1\text{kHz}}$
0, 10, 20 and 30	1	$V_{1\text{kHz}}$	

20	$0.99931 * V_{1\text{kHz}}$	$1.00069 * V_{1\text{kHz}}$
45	$0.99713 * V_{1\text{kHz}}$	$1.00288 * V_{1\text{kHz}}$
100	$0.99083 * V_{1\text{kHz}}$	$1.00925 * V_{1\text{kHz}}$

Initial Test Connection



Note

Initial test connection is same as AI Offset, as shown in **Figure 1** or **Figure 2**.

Verification Procedure

Complete the following procedure to verify the AI flatness accuracy.

Repeat 2 times, once for each channel.

1. Connect the AI channel under test to the Calibrator as shown in **Figure 1** or **Figure 2**.

Repeat 6 times, once for each gain setting.

Repeat 4 times, once for each frequency in **Table 6**.

2. Configure the calibrator to generate an output with the frequency listed in **Table 6** and amplitude listed in **Table 7**.

Table 7: AI Flatness Inputs

Device Gain (dB)	Configuration	Value
	Amplitude (Vrms)	Frequency (Hz)
-20	6.3	1000
-10	6.3	1000
0	6.3	1000

10	2.0	1000
20	0.63	1000
30	0.2	1000

- Configure an AI Voltage channel task using the values in **Table 8**.

Table 8: AI Flatness Verification Configuration

Configuration	Value
Physical channel	<i>Dev_name/aix</i>
Gain*	Gain from Table 6
Coupling	AC
Terminal Configuration	Pseudodifferential
Excitation (IEPE)	0 (A)
Acquisition mode	Finite number of samples
Rate	250000
Samples Per Channel	125000

*Refer to **Table 3** for the maximum and minimum voltages to specify to ensure the specified gain range is used on the module.

- Start the task.
- Acquire the readings with the DUT.
- Calculate the RMS amplitude of the acquired fundamental harmonic. The first measured amplitude represents $V_{1\text{kHz}}$ referenced in **Table 6**. Subsequent test points will be calculated based on $V_{1\text{kHz}}$, as shown in **Table 6**.

As an example, use the Extract Single Tone Information VI to help calculate the RMS. Note that the output of this VI is peak amplitude, and it must be divided by $\sqrt{2}$ to convert to RMS.

- Stop and clear the task.

IEPE Current Verification

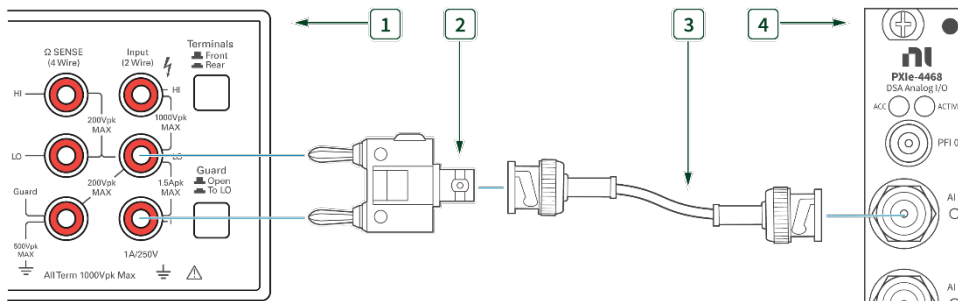
Test Limits

Table 9: IEPE Current Limits

IEPE Current Setting (mA)	As-Found Test Limit	
	Lower Limit (mA)	Upper Limit (mA)
4	3.858	4.205
10	9.655	10.523
20	19.247	20.976

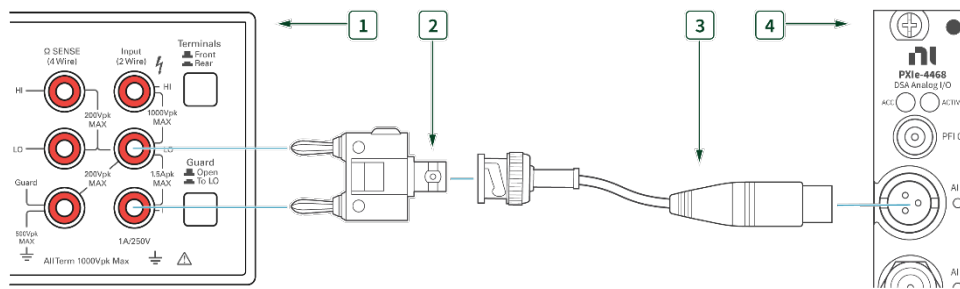
Initial Test Connection

Figure 3. Initial Connection for IEPE Current—BNC



1. DMM
2. Banana - BNC Adapter
3. BNC - BNC Cable
4. PXIe-4468 with BNC

Figure 4. Initial Connection for IEPE Current-mXLR



- 1. DMM
- 2. Banana – BNC Adapter
- 3. BNC – mXLR Cable
- 4. PXIe-4468 with mXLR

Verification Procedure

Complete the following procedure to verify the IEPE current.

Repeat 2 times, once for each channel.

1. Connect the AI channel under test to the DMM as shown in **Figure 3** or **Figure 4**.

Repeat 3 times, once for each IEPE current setting.

2. Set the DMM to the AMPS function and the 10 mA range for the 4 mA and 10 mA test points, and the 100 mA range for the 20 mA test point.
3. Create and configure an AI Voltage task using the values in **Table 10**.

Table 10: IEPE Current Verification Configuration

Configuration	Value
Physical Channels	<i>Dev_name/aix</i>
Gain*	-20 (dB)
Coupling	AC

Terminal Configuration	Pseudodifferential
Excitation (IEPE)	Value from Table 9
Acquisition mode	Finite number of samples
Rate	200000
Samples Per Channel	125000

*Refer to **Table 3** for the maximum and minimum voltages to specify to ensure the specified gain range is used on the module.

4. Start the task.
5. Acquire readings with the DUT. The readings are not used; the task is run to set the device configuration.
6. Measure the output current on the DMM.
7. Stop and clear the task.
8. Compare this value to the limits in **Table 9**.



Note

After the last IEPE current verification step, turn off the current by performing step 3 through 7 with the excitation parameter set to 0.

AO Differential Offset Accuracy Verification

Test Limits

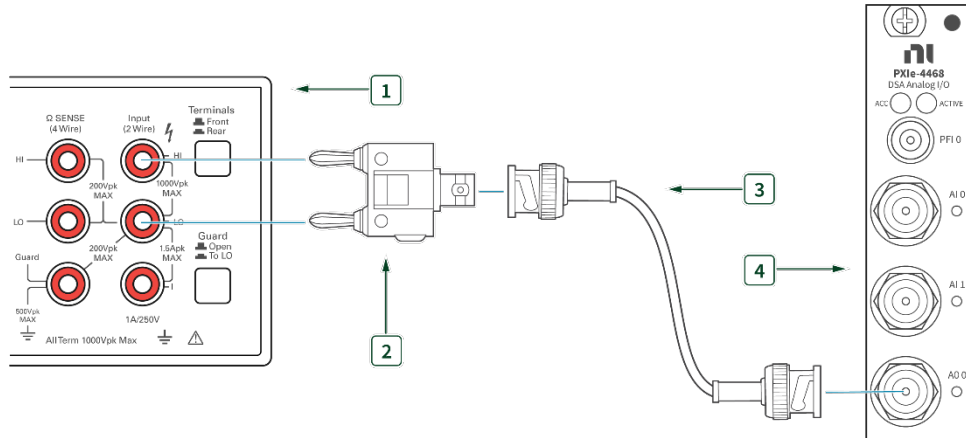
Table 11: AO Differential Offset Verification Limits

AO Attenuation (dB)	As-Found Test Limit		As-Left Test Limit	
	Lower Limit (mV)	Upper Limit (mV)	Lower Limit (mV)	Upper Limit (mV)
0	-1.0	1.0	-0.5	0.5
10	-0.5	0.5	-0.2	0.2
20	-0.2	0.2	-0.1	0.1

30	-0.2	0.2	-0.1	0.1
----	------	-----	------	-----

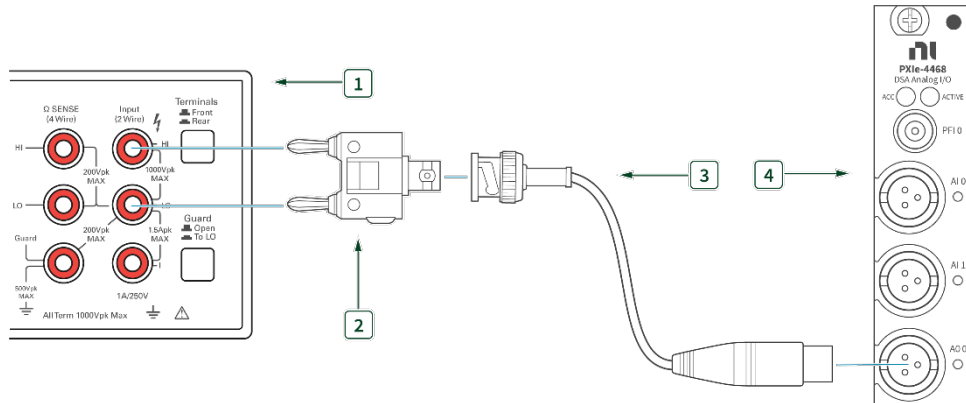
Initial Test Connection

Figure 5. Initial Connection for AO Differential Offset—BNC



1. DMM (Ensure guard to set to LO)
2. Banana – BNC Adapter
3. BNC – BNC Cable
4. PXIe-4468 with BNC

Figure 6. Initial Connection for AO Differential Offset-mXLR



1. DMM (Ensure guard to set to LO)
2. Banana – BNC Adapter
3. BNC – mXLR Cable
4. PXIe-4468 with mXLR

Verification Procedure

Complete the following procedure to verify the AO differential offset accuracy.

Repeat 2 times, once for each channel.

1. Connect the AO channel under test to the DMM as shown in **Figure 5** or **Figure 6**.
2. Configure the DMM using the information in **Table 12**.

Table 12: DMM Configuration

Configuration	Value
Function	DC Volts (DCV)
Range	Fixed - 100 mV
Number of Power Line Cycles (NPLC)	100
MATH NULL	Enabled

Repeat 2 times, once for each output terminal configuration.

Repeat 4 times, once for each AO Attenuation.

3. Configure an AO Voltage channel task using the values in **Table 13**.

Table 13: AO Setup

Configuration	Value
Physical Channels	<i>Dev_name/aox</i>
Output Terminal Configuration	Differential
Rate	200000 S/s
Sample Mode	Continuous Sample
Samples Per Channel	20000
Common-Mode Voltage	0V

4. Set the AO Gain parameter according to the values from **Table 14**.

Table 14: AO Attenuation

AO Attenuation (dB)	AO Gain (dB)
0	0
10	-10
20	-20
30	-30

5. Create an array of 20000 points and fill every element with value 0.
6. Write the array to AO and start the task.
7. Measure the output voltage with the DMM.
8. Stop and clear the task.
9. Compare the result with the limits in **Table 11**.

AO Differential Gain Accuracy Verification

Test Limits

Table 15: AO Differential Gain Verification Limits

Output Terminal Configuration	AO Attenuation (dB)	As-Found Test Limit		As-Left Test Limit	
		Lower Limit (V _{rms})	Upper Limit (V _{rms})	Lower Limit (V _{rms})	Upper Limit (V _{rms})
Differential	0	6.27828	6.32180	6.29710	6.30290
	10	1.99310	2.00692	1.99908	2.0092

	20	0.62783	0.63218	0.62971	0.63029
	30	0.19931	0.20069	0.19991	0.20009
Pseudodifferential	0	6.27828	6.32180	6.28623	6.31380
	10	1.99310	2.00692	1.99563	2.00438
	20	0.62783	0.63218	0.62862	0.63138
	30	0.19931	0.20069	0.19956	0.20044

Initial Test Connection



Note

Initial test connection is same as AO Differential Offset, as shown in **Figure 5** or **Figure 6**.

Verification Procedure

Complete the following procedure to verify the AO differential gain accuracy.

Repeat 2 times, once for each channel.

1. Connect the AO channel under test to the DMM as shown in **Figure 5** or **Figure 6**.

Repeat 2 times, once for each output terminal configuration.

Repeat 4 times, once for each AO Attenuation.

2. Configure the DMM using the information in **Table 16**.

Table 16: DMM Configuration

Configuration	Value
Function	AC Volts (ACV)

Range*	10 V
RMS Mode (SETACV)	3 (SYNC)
AC Bandwidth (ACBAND)	20 Hz
Level Filter (LFILTER)	1 (ON)

*Refer to **Table 17** for details about the correlation between AO Gain, DMM Range, and Signal Amplitude.

Table 17: Setting for AO Gain Verification

AO Attenuation (dB)	AO Gain (dB)	DMM Range (Vrms)	Signal Amplitude (Vpk)
0	0	10	$6.3 * \sqrt{2}$
10	-10	10	$2.0 * \sqrt{2}$
20	-20	1	$0.63 * \sqrt{2}$
30	-30	1	$0.2 * \sqrt{2}$

3. Configure an AO Voltage channel task using the values in **Table 18**.

Table 18: AO Setup

Configuration	Value
Physical Channels	<i>Dev_name/aox</i>
AO Gain*	Gain from Table 17
Output Terminal Configuration	Configuration from Table 15
Rate	200000 S/s
Sample Mode	Continuous Sample
Samples Per Channel	20000

*Refer to **Table 17** for details about the correlation between AO Gain, DMM Range, and Signal Amplitude.

4. Call Basic Function Generator using the parameters in **Table 19**.

Table 19: Basic Function Generator Parameters

Parameter	Value
Signal Type	Sine Wave
Frequency	1000 Hz
Amplitude*	Amplitude from Table 17
Sampling Info>>Sampling Rate	200000 S/s
Sampling Info>>Number of Samples	20000

*Refer to **Table 17** for details about the correlation between AO Gain, DMM Range, and Signal Amplitude.

5. Write the resulting waveform to AO and start the task.
6. Measure the output voltage with the DMM.
7. Stop the task.
8. Compare the result with the limits in **Table 15**.



Note

Before proceeding to the next channel, call DAQmx Channel Property Node, and set the AO Idle Output Behavior property (Analog Output>>General Properties>>Output Configuration>>Idle Output Behavior) to Zero Volts. This will avoid any damage to the device that may be caused by removing cables while the output is active.

AO Gain Flatness Verification

Test Limits

Table 20: AO Gain Flatness Verification Limits

Device Gain (dB)	Output Terminal Configuration	Frequency	As-Found Test Limit	
			Lower Limit (V_{rms})	Upper Limit (V_{rms})
0, 10, 20, and 30	Differential	1 kHz	$V_{1\text{kHz}}$	
		20 kHz	$0.999079 * V_{1\text{kHz}}$	$1.000921 * V_{1\text{kHz}}$
		90.6 kHz	$0.988553 * V_{1\text{kHz}}$	$1.011579 * V_{1\text{kHz}}$
	Pseudodifferential	1 kHz	$V_{1\text{kHz}}$	
		20 kHz	$0.999079 * V_{1\text{kHz}}$	$1.000921 * V_{1\text{kHz}}$
		90.6 kHz	$0.988553 * V_{1\text{kHz}}$	$1.011579 * V_{1\text{kHz}}$

Initial Test Connection



Note

Initial test connection is same as AO Differential Offset, as shown in **Figure 5** or **Figure 6**.

Verification Procedure

Complete the following procedure to verify the AO gain flatness.

Repeat 2 times, once for each channel.

1. Connect the AO channel under test to the DMM as shown in **Figure 5** or **Figure 6**.

Repeat 2 times, once for each output terminal configuration.

Repeat 4 times, once for each AO Attenuation.

Repeat 3 times, once for each frequency.

2. Configure the DMM using the information in **Table 16**.
3. Configure an AO Voltage channel task using the values in **Table 21**.

Table 21: AO Setup

Configuration	Value
Physical Channels	<i>Dev_name/aox</i>
AO Gain*	Gain from Table 20
Output Terminal Configuration	Configuration from Table 20
Rate	200000 S/s
Sample Mode	Continuous Sample
Samples Per Channel	10000

*Refer to **Table 17** for details about the correlation between AO Gain, DMM Range, and Signal Amplitude.

4. Call DAQmx Channel Property Node, and set the AO Idle Output Behavior property (Analog Output>>General Properties>>Output Configuration>>Idle Output Behavior) to Zero Volts
5. Call Basic Function Generator Parameters using the parameters in **Table 22**.

Table 22: Basic Function Generator Parameters

Parameter	Value
Signal Type	Sine Wave
Frequency	1000 Hz
Amplitude*	Amplitude from Table 17
Sampling Info>>Sampling Rate	200000 S/s
Sampling Info>>Number of Samples	10000

*Refer to **Table 17** for details about the correlation between AO Gain, DMM Range, and Signal Amplitude.

6. Write the resulting waveform to AO and start the task.
7. Measure the output voltage with the DMM, and record as $V_{1\text{kHz}}$ for future calculations. The first measured amplitude represents $V_{1\text{kHz}}$ referenced in **Table 20**. Subsequent test points will be calculated based on $V_{1\text{kHz}}$, as shown in **Table 20**.
8. Stop the task.
9. Compare the result with the limits in **Table 20**.

AO Common-Mode Gain and Offset Verification

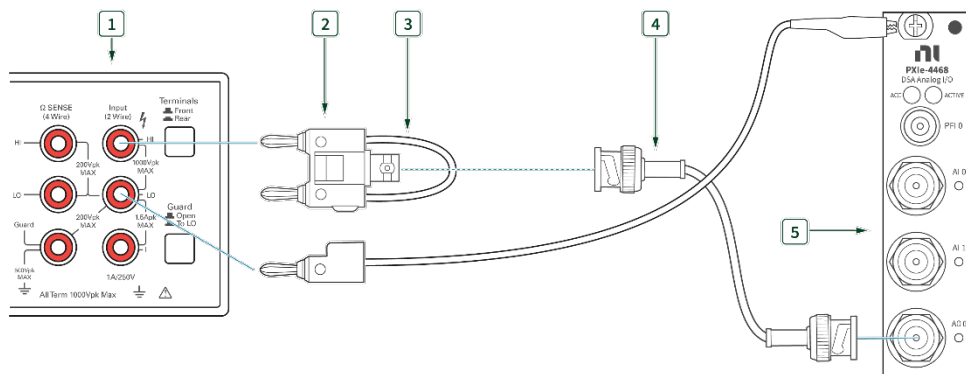
Test Limits

Table 23: AO Common-Mode Gain and Offset Limits

Test Point (V)	As-Found Test Limit		As-Left Test Limit	
	Lower Limit (V)	Upper Limit (V)	Lower Limit (V)	Upper Limit (V)
0	-0.00600	0.00600	-0.00152	0.00152
1	0.99325	1.00675	0.99790	1.00210
2	1.99250	2.00750	1.99732	2.00268
3	2.99175	3.00825	2.99674	3.00326
4	3.99100	4.00900	3.99616	4.00384
5	4.99025	5.00975	4.99558	5.00442

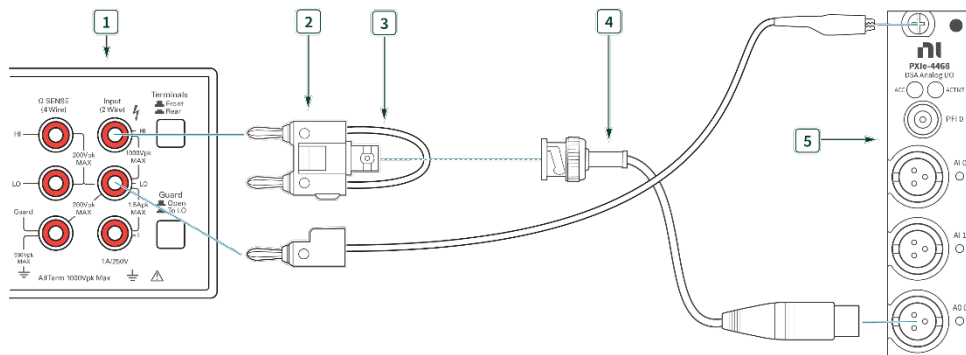
Initial Test Connection

Figure 7. Initial Connection for AO Common-Mode Gain and Offset—BNC



- 1. DMM
- 2. Banana – BNC Adapter
- 3. Shorting Cable (Banana – Banana)
- 4. BNC – BNC Cable
- 5. PXIe-4468 with BNC

Figure 8. Initial Connection for AO Common-Mode Gain and Offset-mXLR



- 1. DMM
- 2. Banana – BNC Adapter
- 3. Shorting Cable (Banana – Banana)
- 4. BNC – mXLR Cable
- 5. PXIe-4468 with mXLR

Verification Procedure

Complete the following procedure to verify common-mode gain and offset.

Repeat 2 times, once for each channel.

- 10. Connect the AO channel under test to the DMM as shown in **Figure 7** or **Figure 8**.

Repeat 6 times, once for each test point.

- 11. Configure the DMM using the information in **Table 12**.

Table 24: DMM Configuration

Configuration	Value
Function	DC Volts (DCV)
Range	Fixed - 10 V
Number of Power Line Cycles (NPLC)	100

MATH NULL

Enabled

12. Configure an AO Voltage channel task using the values in **Table 25**.

Table 25: AO Setup

Configuration	Value
Physical Channels	<i>Dev_name/aox</i>
Output Terminal Configuration	Differential
Rate	200000 S/s
Sample Mode	Continuous Sample
Samples Per Channel	20000
Common-mode voltage	Test Value from Table 23

13. Create an array of 20000 points and fill every element with value 0.
14. Write the array to AO.
15. Start the task.
16. Measure the output voltage on the DMM.
17. Stop and clear the task.
18. Compare this value to the limits in **Table 23**.

Timebase Frequency Accuracy Verification

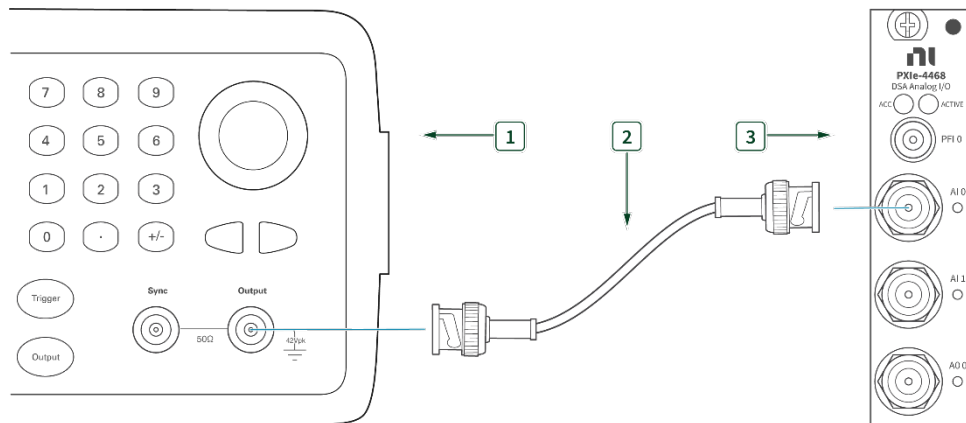
Test Limits

Table 26: Timebase Frequency Accuracy Limits

Function Generator Output		As-Found Test Limit		As-Left Test Limit	
Anplitude (V_{rms})	Frequency (kHz)	Lower Limit (kHz)	Upper Limit (kHz)	Lower Limit (kHz)	Upper Limit (kHz)
6.3	10.000	9.99973	10.00027	9.99992	10.00008

Initial Test Connection

Figure 9. Initial Connection for Timebase Frequency-BNC

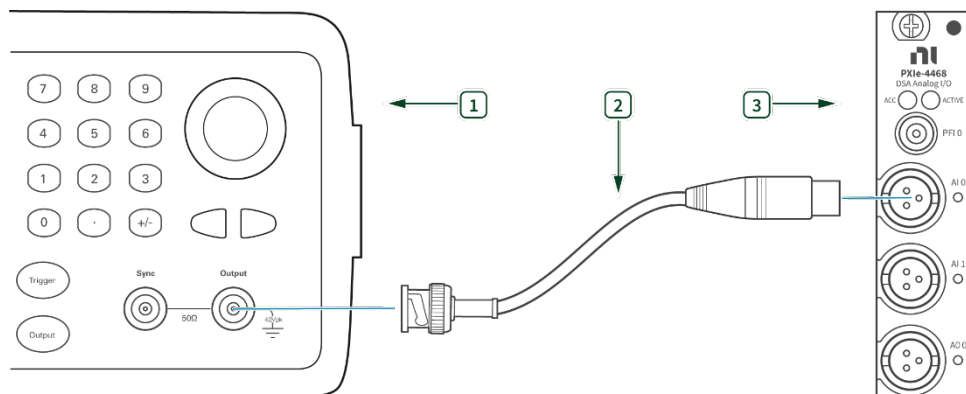


1. Function Generator

3. PXIe-4468 with BNC

2. BNC – BNC Cable

Figure 10. Initial Connection for Timebase Frequency-mXLR



1. Function Generator
2. BNC – mXMLR Cable
3. PXIe-4468 with mXMLR

Verification Procedure



Note

All analog inputs and outputs on a single device use the same timebase circuitry. Therefore, the measurements made on one channel are valid for both channels.

Complete the following procedure to verify the timebase accuracy.

1. Connect the AI channel under test to the function generator as shown in **Figure 9** or **Figure 10**
2. Configure the function generator to output a sine wave of $6.3 V_{rms}$ ($8.9 V_{pk}$) signal, no offset, at a frequency of 10.000 kHz.
3. Create and configure an AI voltage task on the DUT as shown in **Table 27**.

Table 27: Timebase Frequency Verification Configuration

Configuration	Value
Physical Channels	<i>Dev_name/aix</i>
Gain	0 (dB)
Max/Min Voltage	+/-10V
Coupling	AC
Terminal Configuration	Pseudodifferential

Excitation (IEPE)	0 (A)
Acquisition mode	Finite number of samples
Rate	40000.0
Samples per channel	2560000

4. Start the task.
5. Acquire reading with the DUT.
6. Measure the frequency using the Extract Single Tone Information VI of the acquired signal around 10 kHz. Compare the measured frequency to the limits in **Table 27**.
7. Stop and clear the task. Stop generating a signal with the function generator.

Perform Adjustment

AI/AO Gain and Offset Adjustment

Perform an adjustment at least once within the calibration interval. Adjustment automatically updates the calibration constants, the date, and the temperature in the DUT EEPROM. If the DUT passes the verification procedures within the As-Left test limits, an adjustment is not required. Proceed to the *Update the Onboard Calibration Information* section.



Note

Initial test connection is same as AI Offset, as shown in **Figure 1** or **Figure 2**.

Adjustment Procedure

1. Initialization

- Call DAQmxInitExtCal (DAQmx Initialize External Calibration VI) to initialize the calibration using the following parameters:
 - **deviceName:** *Dev_name*
 - **password:** NI
 - **calHandle:** &myCalHandle
2. Connect the calibrator to AI0 as shown in **Figure 1** or **Figure 2**.
 3. Configure the calibrator to generate an output with the amplitude of 6.3 Vrms and frequency of 1kHz.
 4. Call DAQmxAdjust4468Cal (DAQmx Adjust 4468 Calibration VI from the DAQmx Adjust DSA AI Calibration Polymorphic AI), using the following parameters:
 - **calHandle:** myCalHandle
 - **referenceVoltage:** 6.3

Timebase Adjustment

Perform an adjustment at least once within the calibration interval. Adjustment automatically updates the calibration constants, the date, and the temperature in the DUT EEPROM. If the DUT passes the verification procedures within the As-Left test limits, an adjustment is not required. Proceed to the *Update the Onboard Calibration Information* section.



Note

Initial test connection is same as Timebase Frequency Verification, as shown in **Figure 9** or **Figure 10**.

Adjustment Procedure

1. Connect channel AI0 to the function generator as shown in **Figure 9** or **Figure 10**.

2. Configure the function generator to output a sine wave of $6.3 V_{\text{rms}}$ ($8.9 V_{\text{pk}}$) signal, no offset, at a frequency of 90.000 kHz.
3. Call DAQmxAdjustDSADeviceTimebaseCal (DAQmx Adjust DSA Device Timebase Calibration VI) with the following parameters to perform the timebase adjustment:
 - **calHandle:** myCalHandle
 - **referenceFrequency:** 90000.0

Committal Procedure

1. Call DAQmxCloseExtCal (DAQmx Close External Calibration VI) with the following parameters to finish the calibration adjustment:
 - **calHandle:** myCalHandle
 - **action:** DAQmx_Val_Action_Commit or DAQmx_Val_Action_Cancel

Use the action **cancel** if there has been any error during the calibration or if you do not want to save the new calibration constants in the device EEPROM.

Use the action **commit** if you want to save the new calibration constants in the device onboard storage.

Perform Reverification

Perform all tests in the Verification section after completing Adjustment. This verification compares the As-Left limits with measurement data collected after the DUT adjustment. The As-Left limits may be tighter than the As-Found limits.

Update the Onboard Calibration Information

The calibration date can be updated without performing the adjustment procedure. This might be appropriate if the DUT successfully passed each of the verification procedures within the As Left test limits without adjustment. Complete the following steps to update the calibration date:

1. Open a calibration session using the DAQmx Initialize External Calibration VI with the following parameters:
 - **deviceName:** *Dev_name*
 - **password:** NI
 - **calHandle:** &myCalHandle
2. Close the session with the DAQmx Close External Calibration VI with the following parameters:
 - **calHandle:** myCalHandle
 - **action:** DAQmx_Val_Action_Commit

Revision History

Revision	Section	Changes
378817A-01 September 2022	—	This is the initial release version of the PXIe-4468 Calibration Procedure.

NI Services

Visit ni.com/support to find support resources including documentation, downloads, and troubleshooting and application development self-help such as tutorials and examples.

Visit ni.com/services to learn about NI service offerings such as calibration options, repair, and replacement.

Visit ni.com/register to register your NI product. Product registration facilitates technical support and ensures that you receive important information updates from NI.

NI corporate headquarters is located at 11500 N Mopac Expwy, Austin, TX 78759-3504, USA.

Information is subject to change without notice. Refer to the *NI Trademarks and Logo Guidelines* at ni.com/trademarks for more information on National Instruments trademarks. Other product and company names mentioned herein are trademarks or trade names of their respective companies. For patents covering National Instruments products/technology, refer to the appropriate location: **Help»Patents** in your software, the `patents.txt` file on your media, or the *National Instruments Patents Notice* at ni.com/patents. You can find information about end-user license agreements (EULAs) and third-party legal notices in the readme file for your NI product. Refer to the *Export Compliance Information* at ni.com/legal/export-compliance for the National Instruments global trade compliance policy and how to obtain relevant HTS codes, ECCNs, and other import/export data. NI MAKES NO EXPRESS OR IMPLIED WARRANTIES AS TO THE ACCURACY OF THE INFORMATION CONTAINED HEREIN AND SHALL NOT BE LIABLE FOR ANY ERRORS. U.S. Government Customers: The data contained in this manual was developed at private expense and is subject to the applicable limited rights and restricted data rights as set forth in FAR 52.227-14s, DFAR 252.227-7014, and DFAR 252.227-7015.

© 2022 National Instruments Corporation. All rights reserved.

378817A-01 September 2022