Dynamic Signal Acquisition

PXIe-4480/4481 User Manual

6-Channel, 24-bit, 1.25 MS/s DSA Analog Input

October 2016
376368A-01

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Appendix A
NI Services

1 Getting Started

The PXIe-4480 and PXIe-4481 are 6-channel, 24-bit analog input dynamic signal acquisition modules. The modules provide six simultaneously sampled analog input channels and support sample rates of up to 1.25 MS/s per channel in frequency domain mode and 20 MS/s per channel in time domain mode.

The PXIe-4480/4481 modules offer excellent dynamic range, noise and distortion performance, and simultaneous sampling and synchronization capabilities, making them well-suited for many applications including, but not limited to:

- Audio testing
- Acoustic measurements
- Environmental noise testing
- Vibration analysis
- Noise, vibration, and harshness (NVH) measurements
- High speed blast and pressure events
- Underwater transient acoustic measurements

The PXIe-4480 offers a large set of sensor conditioning features, including charge measurement, voltage excitation, IEPE excitation, and TEDS. For applications where the sensors are externally powered, the PXIe-4481 provides the same voltage measurement performance as the PXIe-4480, but without the embedded sensor excitation.

Installation

Refer to the *PXIe-4480/4481 Getting Started Guide* for information about installing, configuring, and setting up the PXIe-4480/4481 Dynamic Signal Acquisition (DSA) analog input module.

Driver support for the PXIe-4480/4481 was first available in NI-DAQmx 16.1. For a list of devices supported by a specific release, refer to the NI-DAQmx Readme, available on the version-specific download page or installation media.

Specifications

Refer to the *PXIe-4480/4481 Specifications* at ni.com/manuals for module specifications.

Accessories

Accessories for the PXIe-4480 and PXIe-4481 include the following shielded InfiniBand 12x cables:

- SHB12X-6BNC (6 BNC analog inputs)
- SHB12X-6MXLRM (6 mini-XLR analog inputs)
- SHB12X-6RJ50 (6 RJ50 analog inputs and voltage excitation)

Refer to ni.com/dsa for information about NI Dynamic Signal Acquisition products and supported accessories.

2

Using the Module

This chapter contains information about configuring and using the PXIe-4480/4481, including information about input connections, signal descriptions, specific features, and fault conditions.

Input Connector Pinouts

The PXIe-4480/4481 front panel has one 73-pin 12x InfiniBand connector. Figure 2-1 and Figure 2-2 show the pinout diagrams for the PXIe-4480 and the PXIe-4481, respectively.

Figure 2-1. PXIe-4480 Pinout

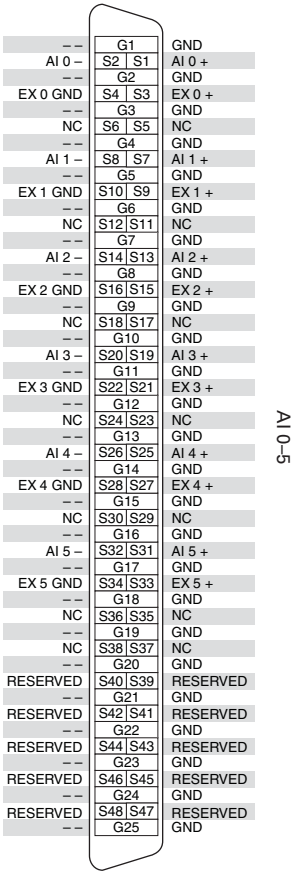
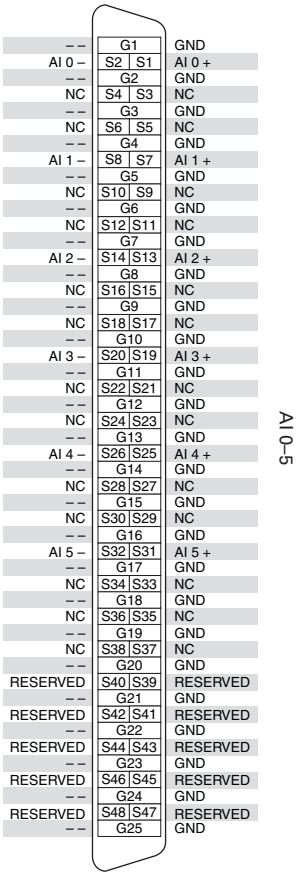


Figure 2-2. PXIe-4481 Pinout



Signal Descriptions

Table 2-1 describes the signals used on the 12x InfiniBand connector.

Table 2-1. Signal Descriptions

Signal Name	Description
AI<0..5>+	Positive input of the differential analog input channels 0 to 5.
AI<0..5>-	Negative input of the differential analog input channels 0 to 5.
EX<0..5>+	Positive terminal of the voltage excitation channels 0 to 5.

Table 2-1. Signal Descriptions (Continued)

Signal Name	Description
EX<0..5> GND	Ground terminal of the voltage excitation channels 0 to 5.
GND	Ground terminal.
NC	Not connected. These pins have no functionality.
RESERVED	Reserved for accessories or other use.

Connecting Signals

Refer to the following tables for connector pin assignments.

Table 2-2. RJ50 Connector Pin Assignments

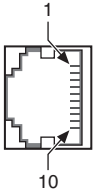
RJ50 Modular Plug Pin Number Diagram	Pin	Signal Name	Signal Description
	1	NC	No connect
	2	AI+	Positive analog input signal (0 to 5)
	3	AI-	Negative analog input signal (0 to 5)
	4	NC	—
	5	NC	—
	6	EX+	Positive excitation (0 to 5), PXIe-4480 only
	7	EX GND	Excitation ground (0 to 5), PXIe-4480 only
	8	NC	—
	9	GND	Ground
	10	NC	—
	Shell	GND	Ground

Table 2-3. BNC Connector Pin Assignments

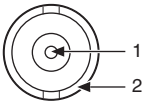
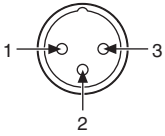
BNC Connector Pin Diagram	Pin	Signal Name	Signal Description
	1	AI+	Positive analog input signal (0 to 5)
	2	AI-	Negative analog input signal (0 to 5)

Table 2-4. mXLR Connector Pin Assignments

mXLR (Male) Connector Pin Diagram	Pin	Signal Name	Signal Description
	1	GND	Chassis ground
	2	AI+	Positive analog input signal (0 to 5)
	3	AI-	Negative analog input signal (0 to 5)
	Shell	GND	Chassis ground

Front Panel LED Status

The PXIe-4480/4481 module uses two LEDs to indicate status and activity. Table 2-5 summarizes the functionality of the LEDs on the module.

Table 2-5. PXIe-4480/4481 LED Descriptions

LED	State	Description
Access	Off	Module is not yet functional, or the module has detected a problem with a power rail.
	Amber	The module is being accessed. The Access LED flashes amber for 75 ms when the module is accessed.
	Green	Module is ready to be accessed by software.
Active	Off	Module is not acquiring or preparing to acquire data.
	Amber	Module is waiting for a trigger event to start an acquisition.
	Green	An acquisition has been triggered, and the module is currently acquiring data.
	Blinking Amber/Green	The module is changing reference clock timebase.
	Steady Red	An error has been detected by hardware. Use NI-DAQmx software to determine the cause and/or clear the error by resetting the module.

Block Diagrams

Figure 2-3 shows the PXIe-4480 analog input circuitry block diagram. Depending on the connector type, connect the signals as described in the *Connecting Signals* section.

Figure 2-3. PXIe-4480 Analog Input Block Diagram

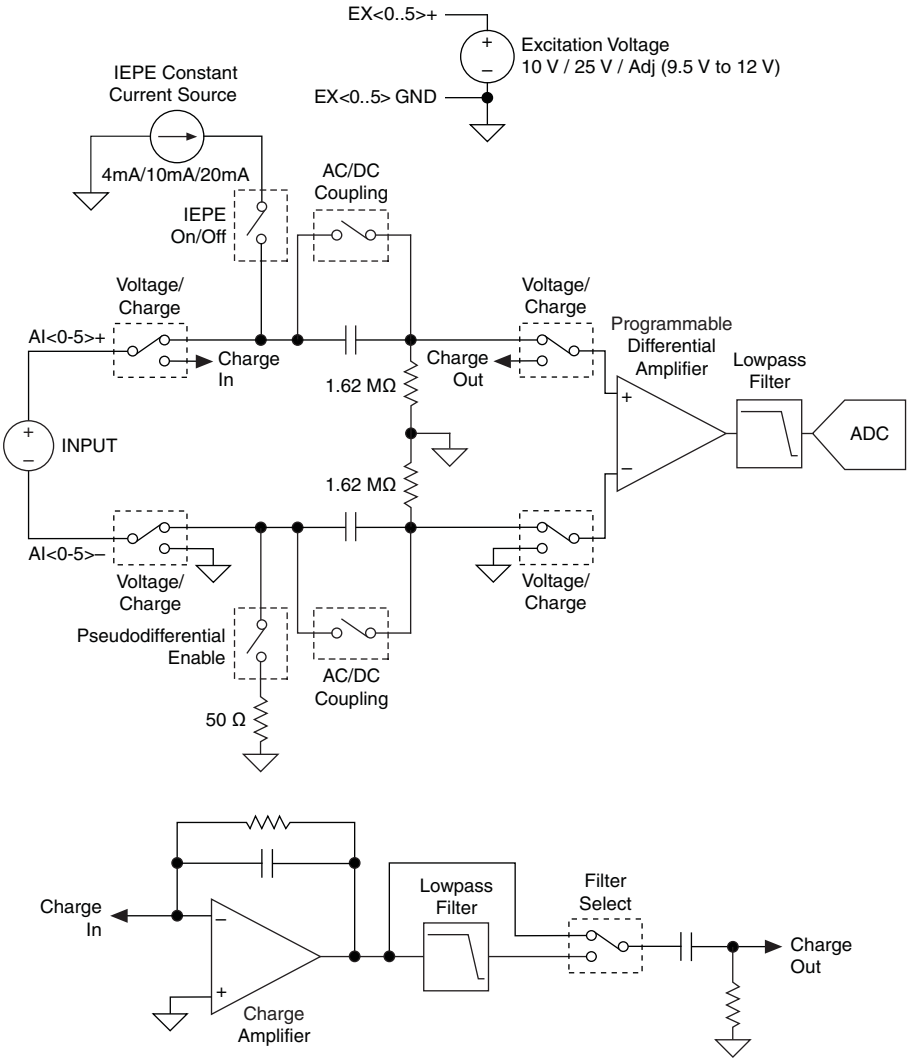
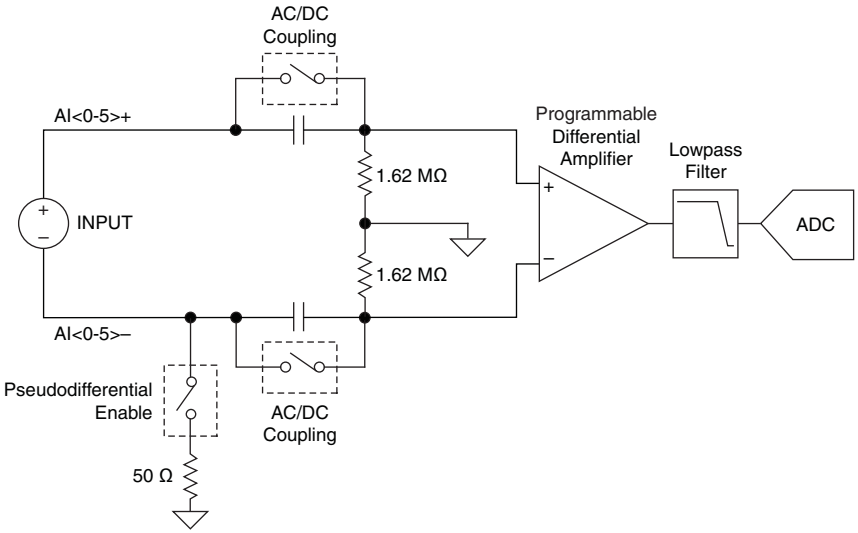


Figure 2-4 shows the PXIe-4481 analog input circuitry block diagram. Depending on the connector type, connect the signals as described in the *Connecting Signals* section.

Figure 2-4. PXIe-4481 Analog Input Block Diagram



Channel Types

The PXIe-4480 and PXIe-4481 support the measurement applications shown in Table 2-6.

Table 2-6. Supported Measurement Applications

Application	PXIe-4480	PXIe-4481
Direct voltage	✓	✓
Voltage-based sensors that are externally powered	✓	✓
IEPE sensors (powered with embedded IEPE current source) including TEDS	✓	
Amplified/powered sensors (powered with embedded voltage excitation source)*	✓	
Charge sensors (measured with embedded charge-to-voltage amplifier)	✓	

* Embedded voltage excitation source is accessible only when using an accessory, such as the SHB12X-6RJ50, that provides access to the excitation terminals.

For maximum flexibility, the module's channel type is programmable on a per-channel basis.

Channel Configuration

The PXIe-4480/4481 supports two terminal configurations for analog voltage input: differential and pseudodifferential. The term *pseudodifferential* refers to the 50 Ω resistance between the negative input terminal and chassis ground.

Note Attach the PXIe-4480/4481 to the chassis with the screws on the top and bottom of the front panel to provide a reliable ground connection.

If the signal source is floating, use the pseudodifferential input configuration. The pseudodifferential configuration provides a ground reference connection for the floating source by connecting a 50 Ω resistor from the negative input to ground. Without this, the floating source can drift outside of the common-mode range of the module.

If the signal source is grounded or ground-referenced, both the pseudodifferential and differential input configurations are acceptable. However, the differential input configuration is preferred, since using the pseudodifferential input configuration on a grounded signal source creates more than one ground reference point. This condition may allow ground loop currents, which can introduce errors or noise into the measurement. The 50 Ω resistor between the negative input and ground is usually low enough to reduce these errors to negligible levels, but results can vary depending on your system setup.

Configure the channels based on the signal source reference or DUT configuration. Refer to Table 2-7 to determine how to configure the channel.

Table 2-7. Channel Configuration

Source Reference	Channel Configuration
Floating	Pseudodifferential
Grounded	Differential or pseudodifferential

For maximum flexibility, the module's input configuration is programmable on a per-channel basis.

Note The differential/pseudodifferential input selection is available for the voltage measurement function. In the charge measurement function (PXIe-4480 only), the negative input terminal is grounded.

Input Connections

Figure 2-5 shows the PXIe-4480/4481 voltage input connection with the terminals in differential configuration.

Figure 2-5. PXIe-4480/4481 Voltage Input Connection in Differential Configuration

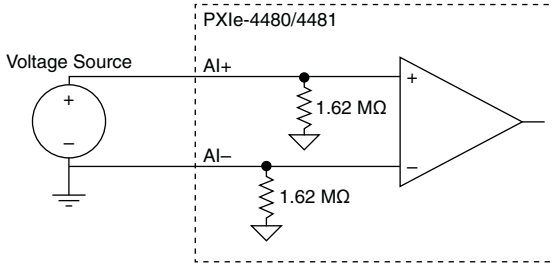


Figure 2-6 shows the PXIe-4480/4481 voltage input connection with the terminals in pseudodifferential configuration.

Figure 2-6. PXIe-4480/4481 Voltage Input Connection in Pseudodifferential Configuration

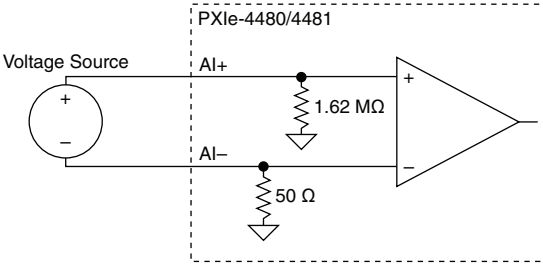
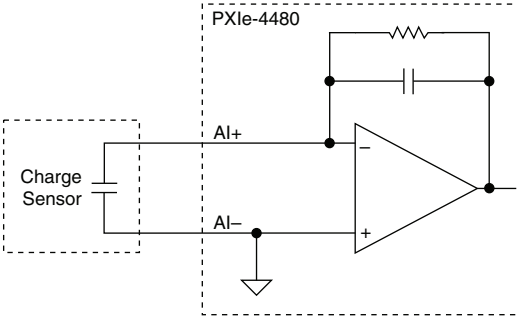


Figure 2-7 shows the PXIe-4480 input connection for the charge mode channel type.

Figure 2-7. PXIe-4480 Charge Input Connection



Refer to the *Measurement System Types and Signal Sources* topic in the *NI-DAQmx Help* for more information about terminal configurations.

Input Coupling

You can configure the PXIe-4480/4481 modules for either AC or DC coupling. If you select DC coupling, any DC offset present in the source signal is passed to the ADC. The DC-coupled configuration is usually best if the signal source has only small amounts of offset voltage or if the DC content of the acquired signal is important. If the source has a significant amount of unwanted offset, select AC coupling to take full advantage of the input dynamic range.

Selecting AC coupling enables a highpass RC filter into the signal conditioning path. Using AC coupling results in an attenuation of the low-frequency response of the AI circuitry. Refer to the *PXIe-4480/4481 Specifications* for information about the cut-off frequency for the device.

For maximum flexibility, the module's input coupling is programmable on a per-channel basis.

IEPE Excitation

The PXIe-4480 provides an integrated electronic piezoelectric (IEPE) excitation current for each channel to measure IEPE or other current-excited sensors. To match a variety of sensor requirements, the current source is configurable with three settings: 4 mA, 10 mA, and 20 mA.

For maximum flexibility, the module's IEPE current selection is programmable on a per-channel basis.

Note Typical IEPE sensors have an enclosure that is electrically isolated from the IEPE electronics. As a result, connecting the sensor to the PXIe-4480 results in a floating connection even though the enclosure of the sensor is grounded.

Transducer Electronic Data Sheet

The PXIe-4480 supports Class 1 Transducer Electronic Data Sheet (TEDS) according to the IEEE 1451.4 standard.

TEDS-capable sensors carry a built-in, self-identification EEPROM that stores a table of parameters and sensor information. TEDS sensors have two modes of operation:

- **Analog mode** allows the sensors to operate as transducers measuring physical phenomena.
- **Digital mode** allows you to write and read information to and from the TEDS.

TEDS contains information about the sensor, such as calibration, sensitivity, and manufacturer information. This information is accessible in Measurement & Automation Explorer (MAX), VIs in LabVIEW, or by calling the equivalent function calls in a text-based ADE.

For more information on TEDS structure and contents, go to `ni.com/info` and enter the Info Code `rdted6`.

Voltage Excitation

The PXIe-4480 provides a programmable voltage excitation source for each channel, designed primarily to interface with powered/amplified sensors. This type of sensor accepts a wide-ranging external power source, regulates it to a voltage suitable for its internal electronics, and provides its signal on amplifier output terminals.

Note The voltage excitation feature is available only when using an accessory, such as the SHB12X-6RJ50, that provides access to the excitation terminals.

Figure 2-8 illustrates the internal construction of a powered/amplified sensor. Table 2-8 provides a guide for connecting signals from the PXIe-4480 to the sensor.

Figure 2-8. Powered/Amplified Sensor

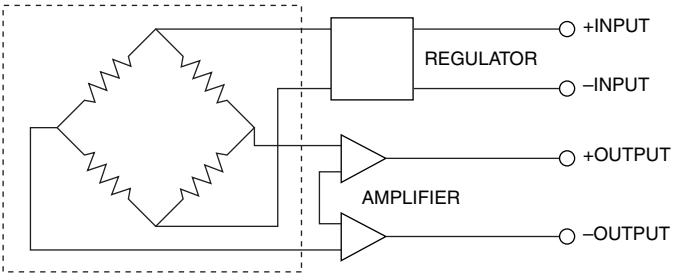


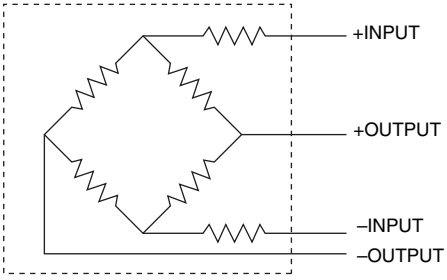
Table 2-8. Powered/Amplified Sensor Connection

Sensor Terminal*	Module Terminal
+INPUT	EX+
-INPUT	EX GND
+OUTPUT	AI+
-OUTPUT	AI-
* Sensor terminal names are for illustrative purposes only and may vary across sensor types and vendors.	

To match a variety of sensor requirements, the voltage source is configurable with two fixed settings: 10 V and 25 V.

It is also possible to utilize the voltage excitation source to excite a passive full-bridge strain gage, as shown in Figure 2-9. Refer to Table 2-8 for a guide to connecting signals from the PXIe-4480 to the strain gage.

Figure 2-9. Full Bridge Strain Gage



Care must be exercised in this type of application, however, as the PXIe-4480 does not provide some of the features of a true strain measurement module, specifically remote sense of the excitation voltage. Without remote sense, the voltage present at the bridge will be slightly less than output by the module, due to the presence of lead wire resistance. Without compensation, this difference would translate into measurement error.

To mitigate this effect, however, the voltage source is adjustable in a nominal range of 9.5 V to 12 V. During initial system setup, the bridge voltage would be externally measured and the voltage source iteratively adjusted until the desired bridge excitation voltage is achieved.

For maximum flexibility, the module's voltage excitation selection is programmable on a per-channel basis.

Fault Conditions

IEPE Open and IEPE Short

When IEPE is enabled, the PXIe-4480 monitors the output voltage to detect if there is a connection issue with the attached signal source. Common connection issues that can occur include open and short circuits. An open circuit occurs if there is a disconnect between the signal source and the module, resulting in the output voltage rising too high. A short circuit occurs if the module inputs have been shorted, for example due to a sensor fault, resulting in the output voltage falling too low. If an open or short event occurs, the hardware will continue to perform the programmed acquisition, but turn the Active LED red and set a flag that can be queried by the user.

Refer to the *Open Current Loop Detection* and *Overcurrent Detection* topics of the *NI-DAQmx Help* for more information on how to use the IEPE Open or IEPE Short feature.

Voltage Excitation Current Limit

When the voltage source is enabled, the PXIe-4480 monitors the output current. If the current exceeds its specified maximum value, the source will continue to operate, but its voltage regulation will be degraded. In addition, the hardware will turn the Active LED red and set a flag that can be queried by the user. Refer to the *Excitation Fault Detection* topic of the *NI-DAQmx Help* for more information on how to use the Voltage Excitation Current Limit detection.

Overtemperature Detection

The PXIe-4480/4481 continuously monitors its ambient temperature. An overtemperature condition is reported when the ambient temperature of the module exceeds a safe operating level. The PXIe-4480/4481 treats overtemperature as a non-fatal error in that the module can still be operated while in this condition. However, the integrity of the data being acquired may be compromised while the PXIe-4480/4481 is displaying an overtemperature condition. If an overtemperature condition is detected, the hardware will turn the Active LED red and set a flag that can be queried by the user. Refer to the *Overtemperature Detection* topic of the *NI-DAQmx Help* for more information on how to determine if an overtemperature condition has occurred.

Refer to your PXI Express chassis specific documentation and the *Maintain Forced-Air Cooling Note to Users* to verify that the chassis spacing requirements and guidelines for adequate cooling of the system are being followed.

3

Signal Acquisition

This chapter contains information about signal acquisition concepts, including analog-to-digital converters, operation modes, filtering, timing, triggering, and synchronization.

Analog-to-Digital Converter

The PXIe-4480/4481 analog-to-digital converters (ADCs) use the Delta-Sigma modulation conversion method. This approach involves oversampling the input signal and then decimating and filtering the resulting data to achieve the desired sample rate.

Nyquist Frequency and Nyquist Bandwidth

Any sampling system, such as an ADC, is limited in the bandwidth of the signals it can measure. Specifically, a sampling rate of *fs* can represent only signals with frequencies lower than *fs*/2.

This maximum frequency is known as the *Nyquist frequency.* The bandwidth from 0 Hz to the Nyquist frequency is the *Nyquist bandwidth*.

Operation Modes

The PXIe-4480/4481 supports two acquisition modes: frequency domain mode and time domain mode.

In a frequency domain mode acquisition, oversampled data is decimated to the requested user sample rate, and digital filters are applied to filter out frequency content above the Nyquist frequency. Frequency domain mode is used any time the requested sample rate is between 100 S/s and 1.25 MS/s. Refer to the *Frequency Domain Mode Acquisitions* section for details on the acquisition process and filters used in frequency domain mode.

The PXIe-4480/4481 also supports time domain mode, in which the oversampled data is loosely filtered so that a maximum amount of bandwidth can be measured. Data may or may not be decimated. Time domain mode is used any time the requested sample rate is above 1.25 MS/s and can operate at up to 20 MS/s. Refer to the *Time Domain Mode Acquisitions* and the *Time Domain Mode Considerations* sections for details on the acquisition process and filters used in time domain mode.

The ability for the module to sample at a requested rate is limited by the module's sample rate generation circuitry and, as a result, a sample rate resolution specification is provided. The sample rate resolution specification indicates how many samples per second are between two adjacent sample rates that the module is capable of producing. Because of the decimation

done by the module, the sample rate resolution improves (becomes smaller) as the sample rate decreases. If a sample rate is requested that the module is not capable of producing exactly, NI-DAQmx software will automatically coerce the sample rate up to the next sample rate that the module is capable of producing. The DAQmx Timing Property Node (**Sample Clock»Rate**) can be used to read the actual sample rate used by hardware.

Frequency Domain Mode Acquisitions

In frequency domain mode, the PXIe-4480/4481 uses a combination of analog and digital filtering to provide an accurate representation of in-band signals while rejecting out-of-band signals. These filters discriminate between signals based on the frequency range, or bandwidth, of the signal. The three important bands to consider are the passband, the stopband, and the alias-free bandwidth. NI-DAQmx uses frequency domain mode automatically any time the requested sample rate is at or below 1.25 MS/s. For sample rates above 1.25 MS/s, time domain mode is always used.

The PXIe-4480/4481 accurately represents signals within the passband, as quantified primarily by passband flatness. All signals that appear in the alias-free bandwidth are either unaliased signals or signals that have been filtered by at least the amount of the stopband rejection.

Anti-Alias Filters

A digitizer or ADC might sample signals containing frequency components above the Nyquist limit. The undesirable effect of the digitizer modulating out-of-band components into the Nyquist bandwidth is aliasing. The greatest danger of aliasing is that you cannot determine if aliasing occurred by looking at the ADC output. If an input signal contains several frequency components or harmonics, some of these components might be represented correctly while others contain aliased artifacts.

Low-pass filtering to eliminate components above the Nyquist frequency either before or during the digitization process can guarantee that the digitized data set is free of aliased components. In frequency domain mode, the PXIe-4480/4481 modules employ both digital and analog low-pass filters to achieve this protection.

In frequency domain mode, the PXIe-4480/4481 modules use an oversampled architecture and sharp digital filters with cut-off frequencies that track the sampling rate. Therefore the filter automatically adjusts to follow the Nyquist frequency. Although the digital filter eliminates almost all out-of-band components, it is still susceptible to aliases from certain narrow frequency bands located at frequencies far above the sampling rate. These frequencies are referred to as the ADC alias holes.

To minimize the error from the ADC alias holes, the PXIe-4480/4481 modules feature a fixed-frequency analog filter. This analog filter removes high-frequency components in the analog signal path before they reach the ADC. This filtering addresses the possibility of high-frequency aliasing from the narrow bands that are not covered by the digital filter.

Passband

The signals within the passband have frequency-dependent gain or attenuation. The small amount of variation in gain with respect to frequency is called the passband flatness. The digital anti-alias filters of the PXIe-4480/4481 adjust the frequency range of the passband to match the sample rate. Therefore, the amount of gain or attenuation at a given frequency depends on the sample rate.

Stopband

The digital anti-alias filter significantly attenuates all signals above the stopband frequency to prevent aliasing. Therefore, the stopband frequency scales precisely with the sample rate. The stopband rejection is the minimum amount of attenuation applied by the anti-alias filter to all signals with frequencies within the stopband.

Alias-Free Bandwidth

Any signal that appears in the alias-free bandwidth of the PXIe-4480/4481 is not an aliased artifact of signals at a higher frequency. The alias-free bandwidth is defined by the ability of the filter to reject frequencies above the stopband frequency, and it is equal to the sample rate minus the stopband frequency.

Filter Group Delay

The anti-alias digital filtering performed by the PXIe-4480/4481 produces a delay of several samples worth of time between when an event occurs on the input signal going into the PXIe-4480/4481 and when the data associated with that event is available at the output of the acquisition and filtering process. This delay is called the group delay. In order to simplify the process of acquiring data from the PXIe-4480/4481 modules and correlating that data with data from other modules, the PXIe-4480/4481 compensates for this group delay in the following ways:

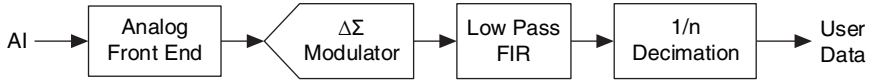
- The Sample Clock output from the PXIe-4480/4481 is generated at the point in time when the input signal is valid at the ADC input pins. When acquiring data, the PXIe-4480/4481 generates a Sample Clock, then waits for the data associated with that Sample Clock to be acquired, then returns that data. As a result, any other acquisitions timed with this Sample Clock line up with the data returned by the PXIe-4480/4481.
- Any triggers generated or received by the PXIe-4480/4481 are interpreted based on their relationship to the Sample Clock being generated. For example, a Start Trigger that starts an acquisition results in data from the next Sample Clock being returned as the first point in the acquisition. Refer to the *Triggering and Filter Delay* section for more details about how this affects analog trigger events.
- On-demand software sampling returns a single sample from an acquisition running at the maximum supported sample rate of the module. For any on-demand, software-timed acquisition the PXIe-4480/4481 waits for the group delay to elapse before returning the sample. As a result, the data returned aligns closely in time with when the data was requested and is delayed by the sum of the analog input delay and digital filter delay.

Time Domain Mode Acquisitions

Time domain mode is an acquisition mode available on the PXIe-4480/4481 which extends the sample rate and bandwidth beyond that of traditional DSA devices. The higher sample rate and bandwidth of time domain mode allows users to measure events in which sudden changes need to be analyzed and understood. These applications include high speed impact, explosive shock, and many others that produce a sharp step response. NI-DAQmx uses time domain mode automatically any time the requested sample rate is above 1.25 MS/s. For sample rates at and below 1.25 MS/s, frequency domain mode is always used.

To allow for higher bandwidth measurements, time domain mode significantly alters the digital signal processing normally done by the Delta-Sigma ADC. Instead of the sharp anti-alias filtering and decimation used in a frequency domain mode, time domain mode uses a single FIR filter applied directly to the Delta-Sigma ADC modulator output. Figure 3-1 illustrates the key processing step involved in a time domain mode acquisition.

Figure 3-1. Time Domain Mode Block Diagram



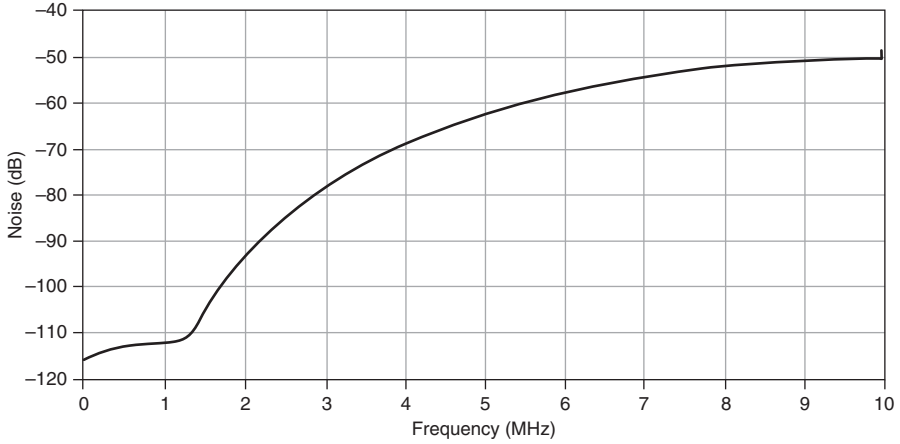
Analog Front End

Before being digitized, the analog input signal is passed through the same analog front end circuitry as in a frequency domain mode acquisition. This means that time domain mode can use all of the same analog channel configurations available on the PXIe-4480/4481. In addition to the channel configuration features, the analog front end also performs anti-alias filtering with respect to the modulator frequency of the Delta-Sigma ADC. The bandwidth of the analog front end and the digital FIR filter combined determine the step response performance of time domain mode.

Delta-Sigma ADC Modulator

After passing through the analog front end for signal conditioning, the signal is digitized by the Delta-Sigma ADC's modulator at a rate of 20 MS/s. In Delta-Sigma ADCs, the modulator is designed to employ a technique called noise shaping. Noise shaping attempts to place all quantization noise above a certain frequency so that digital filtering can be used to remove it. In a frequency domain mode acquisition, this would be done with the sharp anti-alias filters normally found in Delta-Sigma ADCs. In time domain mode, these sharp filters are bypassed and the raw modulator data is sent directly to the FPGA of the PXIe-4480/4481 module where it is filtered. Figure 3-2 shows the FFT power spectrum of the modulator data when the analog inputs are shorted to ground with ±10 V range selected.

Figure 3-2. Delta-Sigma ADC Modulator Noise Power Spectrum



Low Pass FIR Filter

The effect of the modulator noise shaping can be seen above 1.25 MHz. The digital filter removes as much of the modulator noise as possible while still allowing sufficient bandwidth to capture the signal of interest. To illustrate the importance of this, if the digital filter is bypassed (as was done to obtain the modulator noise power spectrum in Figure 3-2), a 400 ns rise time for a 0 V to 10 V step input can be obtained, but the data will have an effective number of bits (ENOB) of 4.2 bits, which makes the acquisition nearly worthless.

The PXIe-4480/4481 can be programmed with a symmetric FIR filter with up to 36 coefficients. Users can design their own filter and, using the NI-DAQmx Channel Property Node, program it to the PXIe-4480/4481. It is required that the filter have the following characteristics:

- Have between 1 and 36 coefficients. Filters larger than 36 coefficients are not allowed due to hardware limitations.
- The filter must be symmetric. This means that a filter with N coefficients must have the first N/2 coefficients match the value of the last N/2 coefficients, but in reverse order. Thus, the first coefficient must be the same value as the last coefficient, the second coefficient must be the same value as the second to last coefficient, and so on. Filters with an odd number of coefficients will have a single coefficient in the middle that does not have a first half/second half match.
- Coefficients must be in the range of 1 to -1.
- The sum of all coefficients should equal (or be very close to) 1. Failure to follow this rule will cause gain errors and in the worst case may result in the DSP math done by the FPGA overflowing and returning invalid data.

If a custom filter is not programmed through the NI-DAQmx Channel Property Node, NI-DAQmx will use a default filter, which is sufficient for most applications. The default time domain mode filter achieves a good balance between the ability to capture high bandwidth events and filtering out modulator noise. Refer to the *PXIe-4480/4481 Specifications* for more information about the default filter and the performance of time domain mode when using the default filter. Step response is affected by both the analog front and the digital filter. Figure 3-3 through Figure 3-6 show full-scale step responses for all four voltage ranges.

Figure 3-3. 10 V Range, Sampled at 20 MS/s

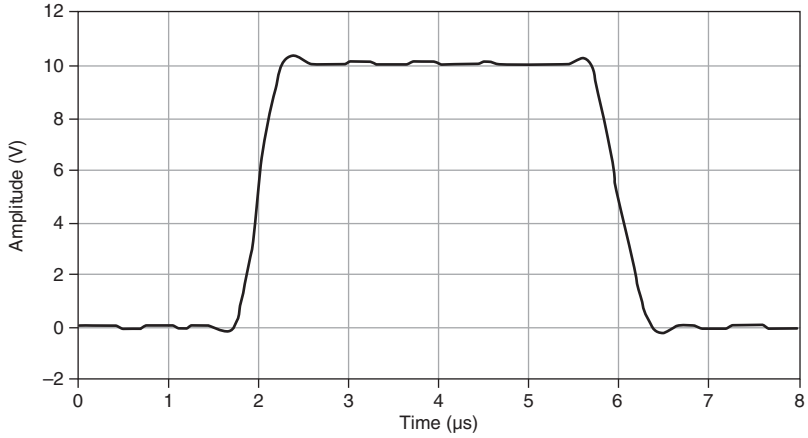


Figure 3-4. 5 V Range, Sampled at 20 MS/s

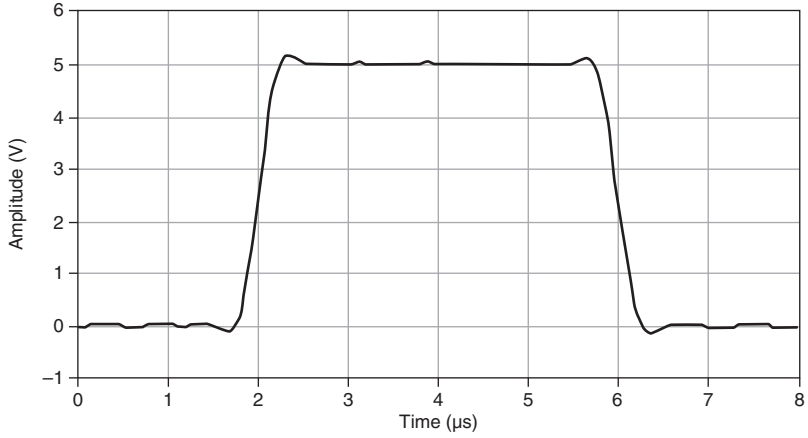


Figure 3-5. 1 V Range, Sampled at 20 MS/s

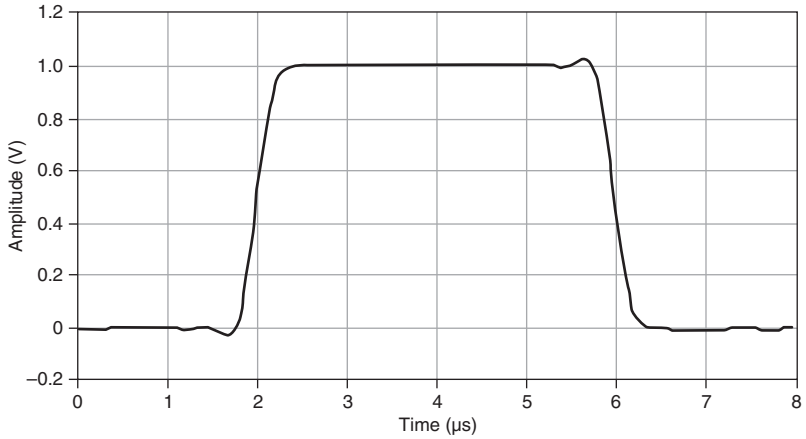
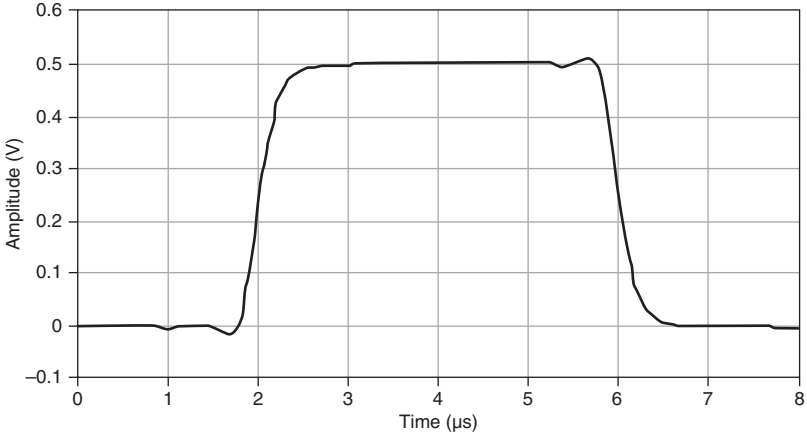


Figure 3-6. 0.5 V Range, Sampled at 20 MS/s



1/n Decimation

Data comes in and out of the digital filter at a rate of 20 MS/s. Depending on the sample rate requested by the user, the filtered data may be decimated by hardware to achieve a slower sample rate than 20 MS/s.

When hardware decimates, it does so by returning every nth sample coming out of the filter. For example, to produce a sample rate of 5 MS/s (n = 4), the hardware drops the first three samples coming from the digital filter and then returns the fourth sample. After sending a sample, the count starts over and the next three samples are dropped before sending the fourth. This pattern

repeats until all requested samples have been sent to the user. The returned samples do not pass through any additional filtering in the decimation process.

The PXIe-4480/4481 supports decimation with n = 1 to 15. The lowest supported rate is 1.333333 MS/s (20 MS/s ÷15). Note that NI-DAQmx always coerces the requested sample rate up to the next sample rate that the hardware is capable of producing. For example, if the requested rate is 1.26 MS/s, NI-DAQmx configures the PXIe-4480/4481 to use time domain mode at 1.333333 MS/s.

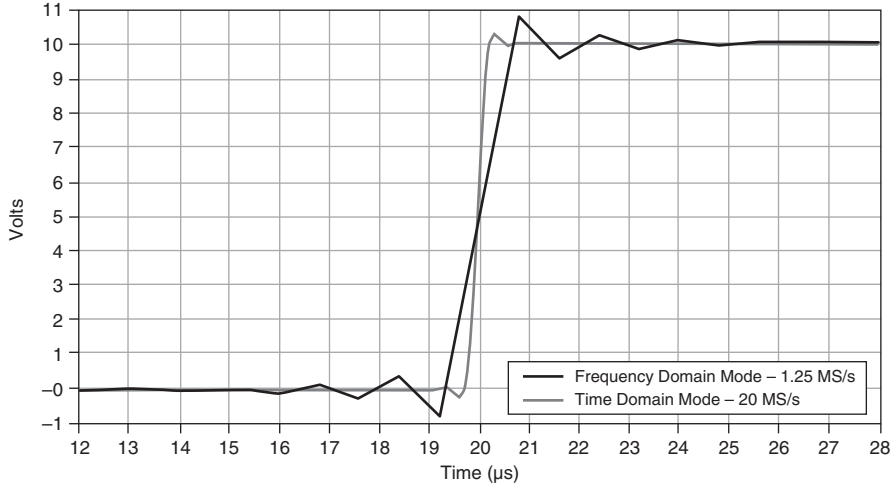
Time Domain Mode Considerations

Comparison to Frequency Domain Mode

Because of the significantly different digital signal processing that occurs after Delta-Sigma modulation, time domain mode has several key differences when compared to frequency domain mode. The following list summarizes these differences.

- Time domain mode is not inherently anti-aliased. Frequency domain mode acquisitions always apply sharp FIR filtering to provide anti-alias rejection regardless of what sample rate is used. In time domain mode, the filter programmed into the digital FIR filter always operates at 20 MS/s regardless of the final rate returned to the user after decimation. Therefore, it is possible for aliasing to occur when using the lower sample rates supported by time domain mode.
- The looser filtering used by time domain mode results in a noisier acquired signal. This is to be expected, as time domain mode allows more bandwidth to come through. In addition, some of the modulation noise that is fully rejected in frequency domain mode is only partially rejected. As a result, the typical ENOB of time domain mode data is roughly 3 bits lower than frequency domain mode sampling at 1.25 MS/s.
- Step responses measured in time domain mode are significantly less distorted than when measured in frequency domain mode. The sharp anti-alias filtering done in frequency domain mode is done with large FIR filters, and for that reason a sudden change in the input produces noticeable ringing before and after the edge as the change propagates through the FIR filtering. The magnitude of this ringing is significantly reduced in time domain mode because of the smaller digital filter applied. Figure 3-7 shows a 0 V to 10 V step as measured in frequency domain mode and in time domain mode. Note that the difference in group delay has been compensated out so that the rising edges overlay.

Figure 3-7. Comparison of Step Response in Frequency Domain and Time Domain Modes



Data Throughput

The amount of data generated by a single PXIe-4480/4481 with all six channels acquiring at 20 MS/s can cause buffer overflow errors if the system is unable to transfer sample data from the device quickly enough. If this occurs, NI-DAQmx software will stop the acquisition and return error -200361, “Onboard device memory overflow…” Buffer overflow errors can be prevented by using data compression and by ensuring the PXI Express system has sufficient data bandwidth.

Data Compression

In normal operation, the PXIe-4480/4481 sends the 24-bit sample data to the host system using 32-bit data words. This means that an additional byte of unused data is transferred for every sample. To improve efficiency, the PXIe-4480/4481 supports packing the sample data so that this unused byte is eliminated. This can be controlled by setting NI-DAQmx Channel Property Node (**Analog Input»General Properties»Advanced»Data Transfer and Memory» Compression»Raw Data Compression Type**) to use lossless packing. The use of lossless packing is required when acquiring 20 MS/s on all six channels continuously, and it is recommended for other configurations to maximize efficiency of system bandwidth resources.

There is, however, a caveat to using lossless packing. Lossless packing requires the total number of samples to be transferred in a finite acquisition to be a multiple of four. The total number of samples to be transferred is equal to the number of acquired samples multiplied by the number of channels used.

For example, if four samples are acquired from two channels, the total number of samples to be transferred is eight, and lossless packing can be used. On the other hand, if three samples are acquired from two channels, then the total number of samples to be transferred is six. Because six is not a multiple of four, an attempt to use lossless packing will cause NI-DAQmx to generate an error.

PXI Express System Bandwidth

In order to continuously transfer large amounts of data, the entire PXI Express system must be designed with sufficient data bandwidth. The PXIe-4480/4481 uses a x4 PXI Express connection to the PXI Express chassis backplane. Note that while the PXIe-4480/4481 will operate with a x1 connection, the amount of data that can be sent to the host computer will be limited and therefore tasks using multiple channels at higher sample rates may experience buffer overflow errors.

Likewise, the bandwidth between the PXI Express chassis and host computer can also limit data throughput. When selecting a PXI Express embedded controller, make sure the controller specifies a sufficient per slot bandwidth (for example, at least 500 MB/s slot bandwidth) and a sufficient system bandwidth to operate all devices installed in the system. If a PXI Express remote controller is selected, it should use a x4 or higher connection. A x1 PXI Express remote controller does not have sufficient bandwidth to allow all channels to acquire at 20 MS/s.

Timing and Triggering

Sample Clock Timebase

The ADCs require an oversample clock to drive the conversion. The oversample clock frequency is greater than the sample rate. On the PXIe-4480/4481 modules, the oversample clock is produced from an 80 MHz reference clock. This 80 MHz reference clock can be phase locked with the PXIe backplane 100 MHz clock, or it can be generated by an internal timebase that runs freely. Multiple modules can be synchronized by selecting the PXIe backplane 100 MHz clock as the reference clock source for all the modules. Refer to the *Reference Clock Synchronization* section for more information.

External Clock

The PXIe-4480/4481 ADCs cannot be clocked from external sources such as encoders or tachometers. However, signal processing features in the Sound and Vibration Measurement Suite often provide an excellent alternative to external clocking in encoder and tachometer applications. Visit `ni.com/soundandvibration` for more information about the Sound and Vibration Measurement Suite.

Timing Engines

When you create a task in software, that software task interacts with a timing engine in the PXIe-4480/4481 hardware. There are a total of three timing engines in hardware that can be operated simultaneously, meaning that three separate tasks can be executed simultaneously, each with different sampling rates and triggering settings. This provides the user with a significant amount of freedom in running multiple sample rates, but there are some limitations:

- The reference clock source must be the same for all tasks, because there is only one reference clock per module.
- A task can only use analog input channels that are not already being used by other tasks.

Digital Triggering

You can configure the PXIe-4480/4481 module to start an acquisition in response to a digital trigger signal from one of the PXI Express backplane trigger lines or the PFI from the front connector. The trigger circuit can respond either to a rising or a falling edge.

Analog Triggering

Analog triggering allows you to trigger your application based on an input signal and trigger level you define. You can configure the analog trigger circuitry to monitor any input channel acquiring data. Choosing an input channel as the trigger channel does not change the input channel acquisition specifications.

The analog trigger signal can be used as a reference trigger only. In a reference-triggered acquisition, you configure the module to acquire a certain number of pre-trigger samples and a certain number of post-trigger samples. Reference-triggered acquisitions can therefore only be configured as finite tasks. The analog trigger on the PXIe-4480/4481 cannot be used as a start trigger. This restriction is a result of the way the module compensates for the filter group delay.

When using an analog reference trigger, the module first waits for the specified number of pre-trigger samples to be acquired. Once enough pre-trigger samples are acquired, the reference trigger will occur the next time the analog trigger condition is met. You also can route the resulting reference trigger event to supported digital terminals. Refer to the **Device Routes** tab in NI-MAX for additional information.

During repetitive triggering on a waveform, you might observe jitter because of the uncertainty of where a trigger level falls compared to the actual digitized data. Although this trigger jitter is usually never greater than one sample period[1], it might be significant when the sample rate is only twice the bandwidth of interest. This jitter usually has no effect on data processing, and you can decrease this jitter by sampling at a higher rate.

You can use several analog triggering modes with the PXIe-4480/4481 modules, including analog edge, analog edge with hysteresis, and window triggering.

[1] For multidevice tasks, trigger jitter when sampling at 20 MS/s may be two sample periods due to hardware limitations. At all other supported sample rates, jitter is never greater than one sample period.

Triggering and Filter Delay

The PXIe-4480/4481 interprets triggers based on where they occur in time. The hardware automatically compensates for its group delay such that data from this module will line up closely in time with the occurrence of the trigger event. However, the group delay affects how long it takes to receive data when starting an acquisition. Since linear phase FIR filters are used in the digital filtering, it is necessary to wait for the filter group delay to elapse after sending a sync pulse before the start trigger can be correctly handled in time. Step 6 in the *Reference Clock Synchronization* section allows NI-DAQmx to handle this delay automatically. After the digital start trigger, you cannot read data for the first sample in software until the digital filter group delay has elapsed. Therefore, it takes a total of twice the digital filter group delay to start an acquisition. You can insert additional time between when the sync pulse occurs and when the start trigger occurs. This will not affect the time it takes before samples are available after the start trigger, which is always the group delay time. Group delay time increases as sample rates decrease.

Synchronization

Some applications require tight synchronization between input and output operations on multiple modules. Synchronization is important to minimize skew between channels and to eliminate clock drift between modules in long-duration operations. You can synchronize the analog input operations on two or more PXIe-4480/4481 modules to extend the channel count for your measurements. In addition, the PXIe-4480/4481 can synchronize with certain DSA modules, such as the PXIe-449x modules, using Reference Clock Synchronization.

Reference Clock Synchronization

With reference clock synchronization, master and slave modules generate their ADC oversample clock from the shared 100 MHz reference clock on the PXIe backplane (PXIe_CLK100). The backplane supplies an identical copy of this clock to each peripheral slot. In addition, multiple chassis can be synchronized by using a timing and synchronization board to lock the 100 MHz clock across chassis.

When you acquire data from multiple modules within the same task, NI-DAQmx will automatically handle all of the Reference Clock Synchronization details required to synchronize the modules within the task. This is known as a Multidevice Task. Refer to the *DSA, SC Express, and X Series Multidevice Tasks* topic in the *NI-DAQmx Help* to determine with which modules the PXIe-4480/4481 can operate in a Multidevice Task.

If a Multidevice Task cannot be used, Reference Clock Synchronization can be done manually. When using multiple NI-DAQmx tasks that are acquiring at the same rate, complete the following steps to synchronize the hardware.

1. Specify PXIe_CLK100 as the reference clock source for all modules to force all the modules to lock to the reference clock on the PXI Express chassis.
2. Choose an arbitrary PXIe-4480/4481 master module to issue a sync pulse on one of the PXIe Trigger lines. The sync pulse resets the ADCs and oversample clocks, phase aligning all the clocks in the system to within nanoseconds.
3. Configure the rest of the modules in your system to receive their sync pulse from the sync pulse master module. This will ensure all ADCs are running in lockstep.
4. Choose one module to be the start trigger master. This does not have to be the same module you chose in step 2.
5. Configure the rest of the modules in your system to receive their start trigger from the start trigger master module. This ensures that all modules will begin returning data on the same sample.
6. Set the synchronization type of the Start Trigger slaves at **DAQmx Trigger»Advanced» Synchronization»Synchronization Type** to Slave and that of the Master to Master.
7. Query **DAQmx Timing»More»Synchronization Pulse»Synchronization Time** on all modules being synchronized, choose the maximum value and set that as the **DAQmx Timing»More»Synchronization Pulse»Minimum Delay To Start** on the module from which the synchronization pulse originates.
8. Commit all of the sync pulse slave module tasks using the DAQmxTaskControl VI/Function. This sets them up to expect the sync pulse from the master.
9. Commit the sync pulse master module task using the DAQmxTaskControl VI/Function. This will issue the sync pulse.
10. Start all of the start trigger slave module tasks. This sets them up to expect the start trigger from the master.
11. Start the start trigger master module task. You can now acquire data.

Tip Consider using a Multidevice task when synchronizing multiple devices at the same rate.

Tip You can find example VIs in the NI Example Finder. Select **Help»Find Examples** to launch the NI Example Finder.

Consider the following caveat to using reference clock synchronization:

- The PXIe-4480/4481 automatically compensates for its filter group delay. However, some other device families do not compensate for their filter delay. In this case, manually compensate for group delay in the waveforms when you synchronize between device families if this level of synchronization is required for your application.

A

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