CALIBRATION PROCEDURE

PXIe-5162

This document contains the verification and adjustment procedures for the PXIe-5162. Refer to *ni.com/calibration* for more information about calibration solutions.

Please review and become familiar with the entire procedure before beginning the calibration process.

Contents

Required Software

Calibrating the PXIe-5162 requires you to install the following software on the calibration system:

- NI-SCOPE 4.0
- Supported application development environment (ADE)—LabVIEW or LabWindows™/CVI™

You can download all required software from *ni.com/downloads*.

Related Documentation

For additional information, refer to the following documents as you perform the calibration procedure:

- *PXIe-5160/5162 Getting Started Guide*
- *NI High-Speed Digitizers Help*
- *PXIe-5162 Specifications*

Visit *ni.com/manuals* for the latest versions of these documents.

Test Equipment

Refer to the following table for a list of necessary equipment and model recommendations for calibration of the PXIe-5162.

If you do not have the recommended equipment, select a substitute calibration standard using the specifications listed in the minimum requirements column of the table.

Table 1. PXIe-5162 Test Equipment

Equipment	Recommended Model	Where Used	Minimum Requirements
Oscilloscope calibrator	Fluke 9500B/600 with Fluke 9530 Active Head	Verifications: • Timebase accuracy • DC accuracy • Input impedance • Input capacitance Adjustment	Sine wave amplitude: 0.9 V pk-pk at 100 MHz into 50 Ω
			Sine wave frequency accuracy: 0.25 ppm at 100 MHz
			Square wave amplitude range: 0.5 V pk-pk to 45 V pk-pk into 1 MΩ, symmetrical to ground (0 V)
			Square wave frequency: 500 Hz
			Square wave aberrations: <2% of peak for the first 500 ns
			DC output range: • ±2.5 V into 50 Ω • ±40 V into 1 MΩ
			DC output accuracy: ±(0.025% of output + 25 µV)
			Impedance measurement: ±0.1% of reading at 50 Ω and 1 MΩ
			Capacitance measurement: ±2% of reading ± 0.25 pF

Table 1. PXIe-5162 Test Equipment (Continued)

Equipment	Recommended Model	Where Used	Minimum Requirements
DMM	NI PXI-4070/4071 or NI PXIe-4081	Verifications: • AC amplitude accuracy	AC voltage accuracy at 50 kHz: • ≤(0.09% of reading + 0.04% of range) for test points < 0.15 V pk-pk • ≤(0.09% of reading + 0.02% of range) for test points ≥ 0.35 V pk-pk
			AC input range: 0.1 V pk-pk to 20 V pk-pk
			AC input impedance: ≥10 MΩ
			Bandwidth: ≥100 kHz
Function generator	NI PXI-5402/5406 or Agilent 33220A	Verifications: • AC amplitude accuracy	Sine wave frequency: 50 kHz
			Sine wave amplitude: • 0.1 V pk-pk to 3.5 V pk-pk into 50 Ω • 0.1 V pk-pk to 20 V pk-pk into 1 MΩ
BNC Tee (m-f-f)	Pasternack PE9174	Verifications: • AC amplitude accuracy	Impedance: 50 Ω
Double banana plug to BNC (f)	Pasternack PE9008	Verifications: • AC amplitude accuracy	Impedance: 50 Ω
BNC (m)-to-BNC (m) cable (x2)	Pasternack PE3087	Verifications: • AC amplitude accuracy	Length: ≤1 meter

Table 1. PXIe-5162 Test Equipment (Continued)

Equipment	Recommended Model	Where Used	Minimum Requirements
Power sensor	Rohde & Schwarz NRP-Z91, NRP6A(N), or NRP18A(N)	Test system characterization Verifications: • Bandwidth	Power range: -26 dBm to 10 dBm
			Frequency range: 50 kHz to 1,500.1 MHz
			Absolute accuracy: • <0.056 dB for 50 kHz to <100 MHz • <0.063 dB for 100 MHz to <1,500.1 MHz
			Relative accuracy at -7 dBm: • <0.023 dB for 50 kHz to <100 MHz • <0.023 dB for 100 MHz to <1,500.1 MHz
			VSWR: ≤1.11:1
Signal generator	Rohde & Schwarz SMA100A or SMA100B	Test system characterization Verifications: • Bandwidth	Frequency range: 50 kHz to 1,500.1 MHz
			Frequency accuracy: ±100.0 ppm
			Amplitude: -20 dBm to 16 dBm
			Harmonics: <-30 dBc

Table 1. PXIe-5162 Test Equipment (Continued)

Equipment	Recommended Model	Where Used	Minimum Requirements
Power splitter[1]	Keysight 11667A or Aeroflex/ Weinschel 1593	Test system characterization Verifications: • Bandwidth	Frequency: 50 kHz to 1,500.1 MHz
			VSWR: ≤1.10:1
50 Ω BNC terminator (f)	Fairview Microwave ST3B-F	Test system characterization	Frequency: DC to 1,500.1 MHz
			VSWR: ≤1.25:1
			Impedance: 50 Ω
50 Ω BNC terminator (m)	Fairview Microwave ST2B	Verifications: • RMS noise	Frequency: DC to 1,500.1 MHz
			VSWR: ≤1.15:1
			Impedance: 50 Ω
Type N (m)-to-Type N (m) cable[2]	Maury Microwave SP-N-MM-24	Test system characterization Verifications: • Bandwidth	Frequency: DC to 1,500.1 MHz
			VSWR: ≤1.10:1
			Length: ≤1 meter
SMA (m)-to-SMA (m) cable[3]	—	Test system characterization Verifications: • Bandwidth	Frequency: DC to 1,500.1 MHz
			VSWR: ≤1.10:1
			Length: ≤1 meter
Type N (m)-to-BNC (m) adapter (×2)[2]	Maury Microwave 8821D1	Test system characterization Verifications: • Bandwidth	Frequency: DC to 1,500.1 MHz
			VSWR: ≤1.08:1

[1] The Aeroflex/Weinschel 1593 must be verified to VSWR ≤1.10:1 from 50 kHz to 1,500.1 MHz. This calibration procedure is written for the Keysight 11667A. If using the Aeroflex/ Weinschel 1593, use the prescribed connectors and adapters in an analogous manner.

[2] Required if using the Keysight 11667A.

[3] Required if using the Aeroflex/Weinschel 1593.

Table 1. PXIe-5162 Test Equipment (Continued)

Equipment	Recommended Model	Where Used	Minimum Requirements
SMA (f)-to-N (m) adapter[3]	Fairview Microwave SM4226	Test system characterization Verifications: • Bandwidth	Frequency: DC to 1,500.1 MHz
			VSWR: ≤1.05:1
			Impedance: 50 Ω
BNC (f)-to-N (f) adapter	Fairview Microwave SM3526	Test system characterization Verifications: • Bandwidth	Frequency: DC to 1,500.1 MHz
			VSWR: ≤1.20:1
			Impedance: 50 Ω
SMA (m)-to-BNC (m) adapter (×2)[3]	Fairview Microwave SM4716	Test system characterization Verifications: • Bandwidth	Frequency: DC to 1,500.1 MHz
			VSWR: ≤1.10:1
			Impedance: 50 Ω
BNC feed-thru terminator	Pomona 4119-50	Verifications: • Bandwidth	Frequency: DC to 300.1 MHz
			VSWR: • ≤1.10:1 at ≤250 MHz • ≤1.20:1 at >250 MHz, ≤301 MHz
			Impedance: 50 Ω

Test Conditions

The following setup and environmental conditions are required to ensure the PXIe-5162 meets published specifications:

- Keep cabling as short as possible. Long cables act as antennas, picking up extra noise that can affect measurements.
- Verify that all connections to the PXIe-5162, including front panel connections and screws, are secure.
- Use shielded copper wire for all cable connections to the module. Use twisted-pair wire to eliminate noise and thermal offsets.

- Maintain an ambient temperature of 23 °C ± 3 °C. The device temperature will be greater than the ambient temperature.
- Keep relative humidity between 10% and 90%, noncondensing.
- Allow a warm-up time of at least 15 minutes after the chassis is powered on and NI-SCOPE is loaded and recognizes the PXIe-5162. The warm-up time ensures that the PXIe-5162 and test instrumentation are at a stable operating temperature.
- Ensure that the PXI chassis fan speed is set to HIGH, that the fan filters, if present, are clean, and that the empty slots contain filler panels. For more information about cooling, refer to the *Maintain Forced-Air Cooling Note to Users* document available at *ni.com/manuals*.
- Plug the chassis and the instrument standard into the same power strip to avoid ground loops.

Password

The default password for password-protected operations is `NI`.

Calibration Interval

Recommended calibration interval	2 years

As-Found and As-Left Limits

The as-found limits are the published specifications for the PXIe-5162. NI uses these limits to determine whether the PXIe-5162 meets the specifications when it is received for calibration. Use the as-found limits during initial verification.

The as-left calibration limits are equal to the published NI specifications for the PXIe-5162, less guard bands for measurement uncertainty, temperature drift, and drift over time. NI uses these limits to reduce the probability that the instrument will be outside the published specification limits at the end of the calibration cycle. Use the as-left limits when performing verification after adjustment.

Calibration Overview

Install the device and configure it in NI Measurement & Automation Explorer (MAX) before calibrating.

Calibration includes the following steps:

1. Self-calibration—Adjust the self-calibration constants of the device.
2. Test system characterization—Characterize the amplitude balance of the output ports on your power splitter. The results of this step are used as a correction in the bandwidth verification procedure.

3. Verification—Verify the existing operation of the device. This step confirms whether the device is operating within the published specification prior to adjustment.
4. Adjustment—Perform an external adjustment of the calibration constants of the device. The adjustment procedure automatically stores the calibration date and temperature on the EEPROM to allow traceability.
5. Re-verification—Repeat the Verification procedure to ensure that the device is operating within the published specifications after adjustment.

Test System Characterization

The following procedures characterize the test equipment used during verification.

Notice The connectors on the device under test (DUT) and test equipment are fragile. Perform the steps in these procedures with great care to prevent damaging any DUTs or test equipment.

Zeroing the Power Sensor

1. Ensure that the power sensor is not connected to any signals.
2. Zero the power sensor using the built-in function, according to the power sensor documentation.

Characterizing Power Splitter Amplitude Balance

This procedure characterizes the amplitude balance of the two output ports of the power splitter over a range of frequencies.

The results of the characterization are later used as a correction in *Verifying 50 Ω Bandwidth* on page 22 and *Verifying 1 MΩ Bandwidth* on page 26.

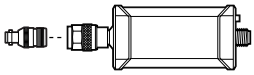
Table 2. Power Splitter Characterization

Config	Test Point	
	Frequency (MHz)	Amplitude (dBm)
1	0.05	-0.5
2	250.1	-0.5
3	300.1	-0.5
4	1,500.1	-0.5

1. Connect the BNC (f)-to-Type N (f) adapter to the power sensor.

   Refer to this assembly as the *power sensor*.

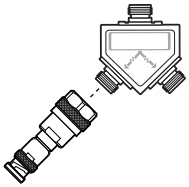
Figure 1. Power Sensor



2. Zero the power sensor as described in the *Zeroing the Power Sensor* section.
3. Connect the RF OUT connector of the signal generator to the input port of the power splitter using a Type N (m)-to-Type N (m) cable.
4. Connect a Type N (m)-to-BNC (m) adapter to one of the power splitter output ports.

   Refer to this assembly as *splitter output 1*.

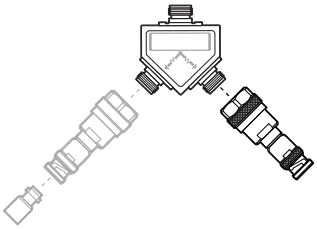
Figure 2. Splitter Output 1



5. Connector the 50 Ω BNC (f) terminator to splitter output 1.
6. Connect the other Type N (m)-to-BNC (m) adapter to the other output port of the power splitter.

   Refer to this assembly as *splitter output 2*.

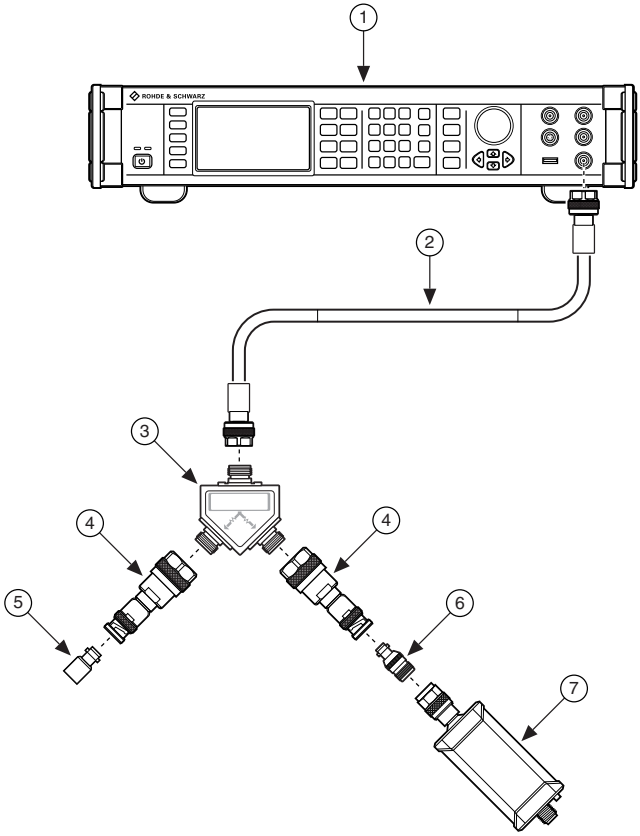
Figure 3. Splitter Output 2



7. Connect the power sensor to splitter output 2.

   The following figure illustrates the hardware setup.

Figure 4. Connection Diagram for Measuring at Splitter Output 2



1. Signal generator
2. Type N (m)-to-Type N (m) cable
3. Keysight 11667A power splitter
4. Type N (m)-to-BNC (m) adapter
5. 50 Ω BNC (f) terminator
6. Type N (f)-to-BNC (f) adapter
7. Power sensor

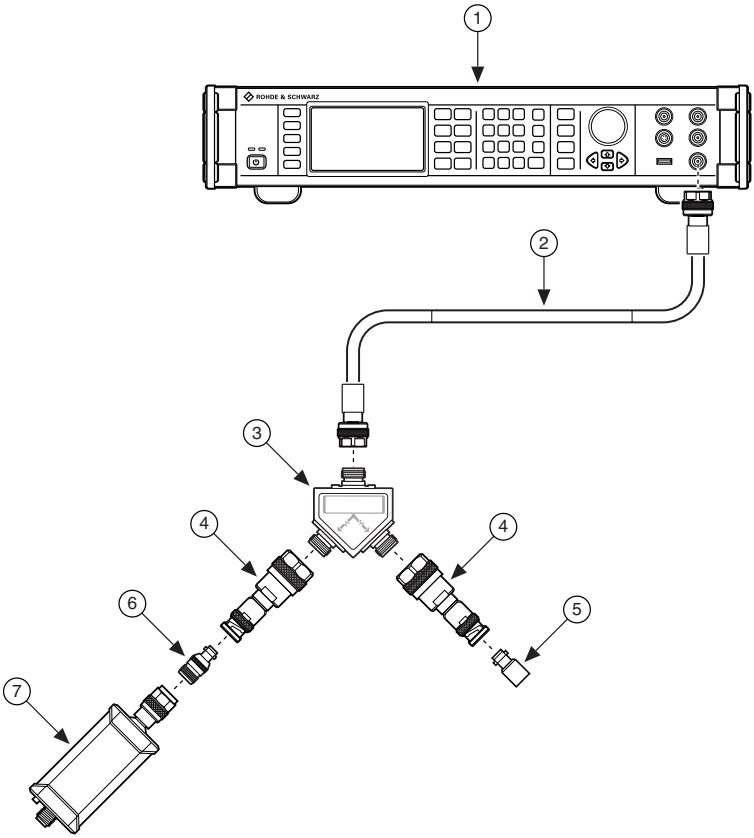
8. Configure the signal generator to generate a sine waveform with the following characteristics:
   - Frequency: the *Test Point Frequency* value from the *Power Splitter Characterization* table
   - Amplitude level: the *Test Point Amplitude* value from the *Power Splitter Characterization* table
9. Configure the power sensor to correct for the *Test Point Frequency* value using the power sensor frequency correction function.
10. Use the power sensor to measure the power in dBm.

    Record the result as *Splitter Output 2 Power*, where each configuration of the power sensor has a corresponding *Splitter Output 2 Power* value.

11. Repeat steps *8* on page 11 through *10* on page 11 for each configuration in the *Power Splitter Characterization* table.
12. Disconnect the power sensor and 50 Ω BNC (f) terminator from splitter output 2 and splitter output 1.
13. Connect the power sensor to splitter output 1.
14. Connect the 50 Ω BNC (f) terminator to splitter output 2.

The following figure illustrates the hardware setup.

Figure 5. Connection Diagram for Measuring at Splitter Output 1



1. Signal generator
2. Type N (m)-to-Type N (m) cable
3. Keysight 11667A power splitter
4. Type N (m)-to-BNC (m) adapter
5. 50 Ω BNC (f) terminator
6. Type N (f)-to-BNC (f) adapter
7. Power sensor

15. Configure the signal generator to generate a sine waveform with the following characteristics:
    - Frequency: the *Test Point Frequency* value from the *Power Splitter Characterization* table
    - Amplitude level: the *Test Point Amplitude* value from the *Power Splitter Characterization* table
16. Configure the power sensor to correct for the *Test Point Frequency* value using the power sensor frequency correction function.
17. Use the power sensor to measure the power in dBm.

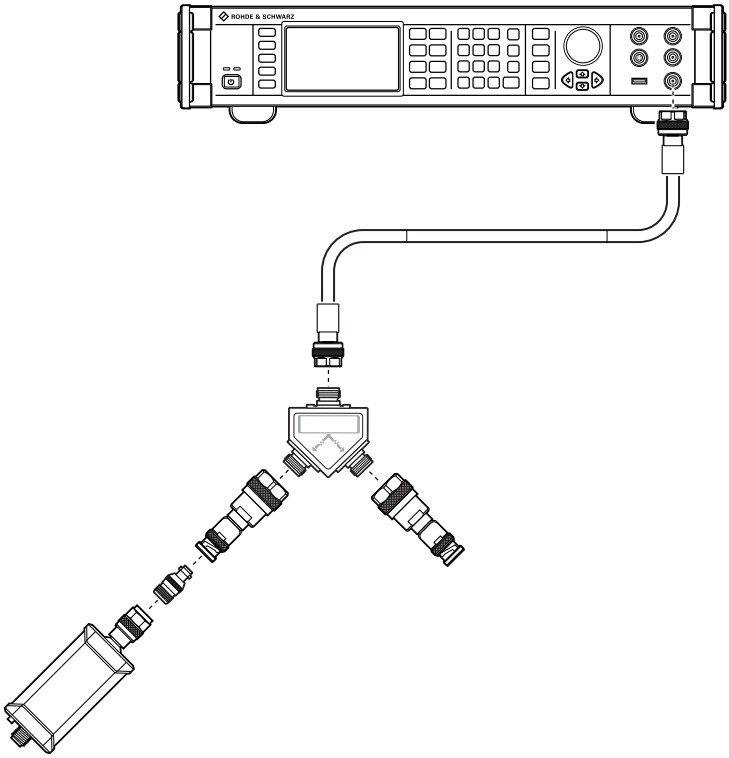
    Record the result as *Splitter Output 1 Power*, where each configuration of the power sensor has a corresponding *Splitter Output 1 Power* value.
18. Repeat steps *15* on page 13 through *17* on page 13 for each configuration in the *Power Splitter Characterization* table.
19. Calculate the splitter balance for each frequency point using the following equation:

    Splitter Balance = Splitter Output 2 Power - Splitter Output 1 Power
20. Disconnect the 50 Ω BNC (f) terminator from splitter output 2.

    Refer to the remaining assembly as the *power sensor assembly*.

Note Do not disassemble the power sensor assembly. The power splitter amplitude balance characterization is invalid if the power sensor assembly has been disassembled.

Figure 6. Power Sensor Assembly



The power sensor assembly will be used in *Verifying 50 Ω Bandwidth* on page 22 and *Verifying 1 MΩ Bandwidth* on page 26.

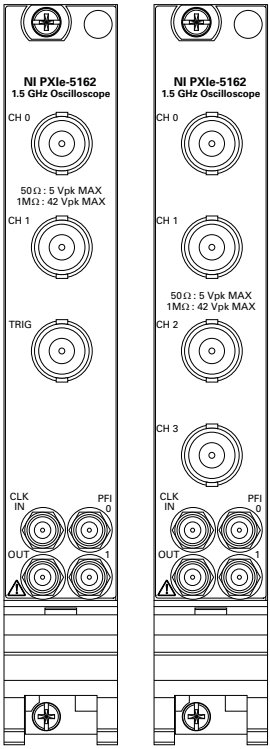
Verification

This section provides instructions for verifying the PXIe-5162 specifications.

Verification of the PXIe-5162 is complete only after you have successfully completed all tests in this section using the *As-Found Limits*.

Refer to the following figure for the names and locations of the PXIe-5162 front panel connectors. You can find information about the functions of these connectors in the device getting started guide.

Figure 7. PXIe-5162 (2 CH) and PXIe-5162 (4 CH) Front Panels



Note The performance verification procedures assume that adequate traceable uncertainties are available for the calibration references.

Verifying DC Accuracy

This procedure verifies the DC accuracy of the PXIe-5162 by comparing the voltage measured by the device to the value sourced by the voltage standard.

Refer to the following table as you complete the following steps.

Table 3. DC Accuracy Verification

Config	Input Impedance (Ω)	Vertical Range (V pk-pk)	Vertical Offset (V)	Test Points (V)	As-Found Limits (mV)	As-Left Limits (mV)
1	50	0.2 V	0	0.090	±3.6	±2.11
2	50	0.2 V	0	-0.090	±3.6	±2.11

Table 3. DC Accuracy Verification (Continued)

Config	Input Impedance (Ω)	Vertical Range (V pk-pk)	Vertical Offset (V)	Test Points (V)	As-Found Limits (mV)	As-Left Limits (mV)
3	50	0.2 V	0.5	0.590	±10.6	±4.16
4	50	0.2 V	-0.5	-0.590	±10.6	±4.16
5	50	0.5 V	0	0.225	±8.1	±4.39
6	50	0.5 V	0	-0.225	±8.1	±4.39
7	50	0.5 V	0.5	0.725	±15.1	±6.44
8	50	0.5 V	-0.5	-0.725	±15.1	±6.44
9	50	1 V	0	0.450	±15.6	±8.57
10	50	1 V	0	-0.450	±15.6	±8.57
11	50	1 V	0.5	0.950	±22.6	±10.62
12	50	1 V	-0.5	-0.950	±22.6	±10.62
13	50	2 V	0	0.900	±30.6	±15.20
14	50	2 V	0	-0.900	±30.6	±15.20
15	50	2 V	1.5	2.400	±51.6	±20.90
16	50	2 V	-1.5	-2.400	±51.6	±20.90
17	50	5 V	0	2.250	±75.6	±40.35
18	50	5 V	0	-2.250	±75.6	±40.35
19	1 M	0.2 V	0	0.090	±3.6	±2.73
20	1 M	0.2 V	0	-0.090	±3.6	±2.73
21	1 M	0.2 V	0.5	0.590	±10.6	±8.23
22	1 M	0.2 V	-0.5	-0.590	±10.6	±8.23
23	1 M	0.5 V	0	0.225	±8.1	±6.08
24	1 M	0.5 V	0	-0.225	±8.1	±6.08
25	1 M	0.5 V	0.5	0.725	±15.1	±11.58
26	1 M	0.5 V	-0.5	-0.725	±15.1	±11.58

Table 3. DC Accuracy Verification (Continued)

Config	Input Impedance (Ω)	Vertical Range (V pk-pk)	Vertical Offset (V)	Test Points (V)	As-Found Limits (mV)	As-Left Limits (mV)
27	1 M	1 V	0	0.450	±15.6	±12.36
28	1 M	1 V	0	-0.450	±15.6	±12.36
29	1 M	1 V	0.5	0.950	±22.6	±17.86
30	1 M	1 V	-0.5	-0.950	±22.6	±17.86
31	1 M	2 V	0	0.900	±30.6	±23.12
32	1 M	2 V	0	-0.900	±30.6	±23.12
33	1 M	2 V	5	5.900	±100.6	±78.12
34	1 M	2 V	-5	-5.900	±100.6	±78.12
35	1 M	5 V	0	2.250	±75.6	±57.30
36	1 M	5 V	0	-2.250	±75.6	±57.30
37	1 M	5 V	5	7.250	±145.6	±112.30
38	1 M	5 V	-5	-7.250	±145.6	±112.30
39	1 M	10 V	0	4.500	±150.6	±119.60
40	1 M	10 V	0	-4.500	±150.6	±119.60
41	1 M	10 V	5	9.500	±220.6	±174.60
42	1 M	10 V	-5	-9.500	±220.6	±174.60
43	1 M	20 V	0	9.000	±300.6	±231.20
44	1 M	20 V	0	-9.000	±300.6	±231.20
45	1 M	20 V	30	39.000	±720.6	±561.20
46	1 M	20 V	-30	-39.000	±720.6	±561.20
47	1 M	50 V	0	22.500	±750.6	±573.00
48	1 M	50 V	0	-22.500	±750.6	±573.00
49	1 M	50 V	15	37.500	±960.6	±738.00
50	1 M	50 V	-15	-37.500	±960.6	±738.00

1. Connect the calibrator test head to channel 0 of the PXIe-5162.

2. Configure the PXIe-5162 with the following settings:
   - Input impedance: the *Input Impedance* value from the *DC Accuracy Verification* table
   - Maximum input frequency: (1 MΩ) 300 MHz, (50 Ω) 1,500 MHz
   - Vertical offset: the *Vertical Offset* value from the *DC Accuracy Verification* table
   - Vertical range: the *Vertical Range* value from the *DC Accuracy Verification* table
   - Sample rate: 5.0 GS/s
   - Minimum number of points: 50,000 samples
   - NI-SCOPE scalar measurement: Voltage Average
3. Configure the calibrator output impedance to match the impedance of the PXIe-5162.
4. Configure the calibrator to output the *Test Point* value from the *DC Accuracy Verification* table.
5. Enable the calibrator output.
6. Wait one second for settling, then record the measured voltage.
7. Use the following formula to calculate the voltage error:

   $DC\ Voltage\ Error = V_{Measured} - Test\ Point$
8. Compare the voltage error to the appropriate limit from the *DC Accuracy Verification* table.
9. Change the maximum input frequency to 175 MHz and repeat steps *6* on page 18 through *8* on page 18.
10. Change the maximum input frequency to 20 MHz and repeat steps *6* on page 18 through *8* on page 18.

    Note If you are calibrating the PXIe-5162 (4 CH), skip the following step for input channels 1 and 3.
11. Configure the device with the following settings and repeat steps *6* on page 18 through *10* on page 18:
    - Maximum input frequency: (1 MΩ) 300 MHz, (50 Ω) 1,500 MHz
    - Sample rate: 2.5 GS/s
12. Configure the device with the following settings and repeat steps *6* on page 18 through *10* on page 18:
    - Maximum input frequency: (1 MΩ) 300 MHz, (50 Ω) 1,500 MHz
    - Sample rate: 1.25 GS/s
13. Repeat steps *2* on page 18 through 12 for each configuration listed in the *DC Accuracy Verification* table.
14. Connect the calibrator test head to channel 1 of the PXIe-5162 and repeat steps *2* on page 18 through 12 for each configuration listed in the *DC Accuracy Verification* table.

    Note If you are verifying the PXIe-5162 (4 CH), proceed to the following step. If you are verifying the PXIe-5162 (2 CH), DC accuracy verification is complete.

15. Connect the calibrator test head to channel 2 of the PXIe-5162 and repeat steps *2* on page 18 through 12 for each configuration listed in the *DC Accuracy Verification* table.
16. Connect the calibrator test head to channel 3 of the PXIe-5162 and repeat steps *2* on page 18 through 12 for each configuration listed in the *DC Accuracy Verification* table.

Verifying AC Amplitude Accuracy

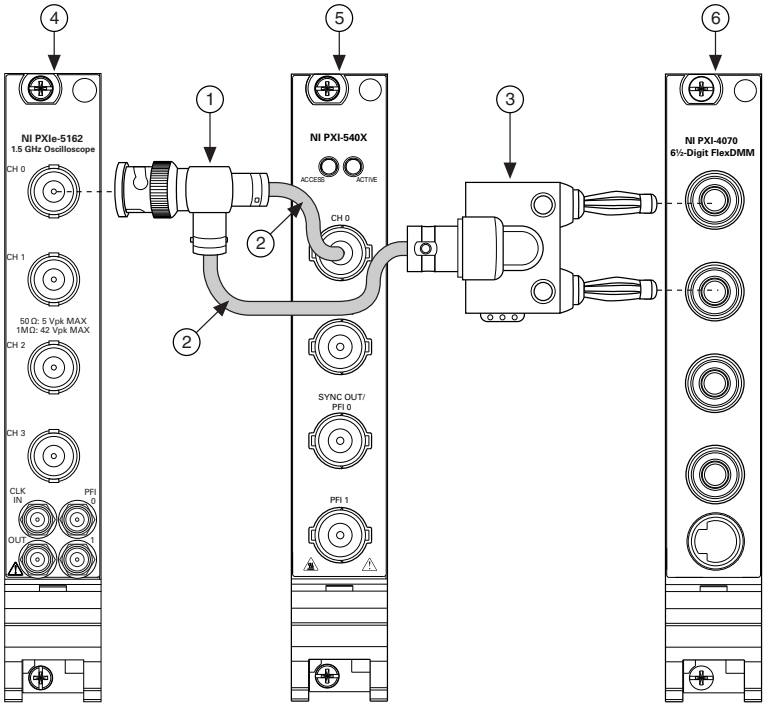
Follow this procedure to verify the AC amplitude accuracy of the PXIe-5162 by comparing the voltage measured by the PXIe-5162 to the voltage measured by the DMM.

Refer to the following table as you complete the following steps:

Table 4. AC Amplitude Accuracy Verification

Config	Input Impedance (Ω)	Vertical Range (V pk-pk)	Test Point (V pk-pk)	Frequency (kHz)	DMM Range (V RMS)	As-Found Limits (dB)	As-Left Limits (dB)
1	50	0.2 V	0.14	50.0	0.05	±0.50	±0.39
2	50	0.5 V	0.35	50.0	0.5	±0.50	±0.39
3	50	1 V	0.7	50.0	0.5	±0.50	±0.39
4	50	2 V	1.4	50.0	0.5	±0.50	±0.39
5	50	5 V	3.5	50.0	5.0	±0.50	±0.39
6	1 M	0.2 V	0.14	50.0	0.05	±0.50	±0.41
7	1 M	0.5 V	0.35	50.0	0.5	±0.50	±0.41
8	1 M	1 V	0.7	50.0	0.5	±0.50	±0.41
9	1 M	2 V	1.4	50.0	0.5	±0.50	±0.41
10	1 M	5 V	3.5	50.0	5.0	±0.50	±0.41
11	1 M	10 V	7	50.0	5.0	±0.50	±0.41
12	1 M	20 V	14	50.0	5.0	±0.50	±0.41
13	1 M	50 V	20	50.0	50.0	±0.50	±0.41

Figure 8. AC Verification Test Connections



1. BNC tee (m-f-f)
2. BNC (m)-to-BNC (m) cable
3. Double banana plug to BNC (f)
4. PXIe-5162
5. Function generator
6. DMM

1. Connect the DMM and function generator to channel 0 of the PXIe-5162 as shown in the *AC Verification Test Connections* figure.
2. Configure the DMM with the following settings:
   - Function: AC voltage
   - Resolution: 6.5 digits
   - Min frequency: 49 kHz
   - Auto Zero: Enabled
   - Range: the *DMM Range* value from the *AC Amplitude Accuracy Verification* table
3. Configure the PXIe-5162 with the following settings:
   - Input impedance: the *Input Impedance* value from the *AC Amplitude Accuracy Verification* table
   - Maximum input frequency: (1 MΩ) 300 MHz, (50 Ω) 1,500 MHz
   - Vertical offset: 0 V
   - Vertical range: the *Vertical Range* value from the *AC Amplitude Accuracy Verification* table

- Sample clock timebase source: VAL_INTERNAL_TIMEBASE
- Sample rate: 2.5 GS/s
- Sample clock timebase multiplier: 4
- Sample clock timebase divisor: 400
- Minimum number of points: 50,000 samples
- NI-SCOPE scalar measurement: AC Estimate

Note The actual sample rate of the PXIe-5162 is calculated by the following formula:
25 MS/s = (*Sample Clock Timebase Rate* × *Sample Clock Timebase Multiplier)* / *Sample Clock Timebase Divisor*

Note Setting the sample clock timebase attribute keeps the PXIe-5162 in the desired configuration even when data decimation is needed to measure the amplitude of the 50 kHz sine wave.

4. Configure the function generator and generate a waveform with the following characteristics:
   - Waveform: sine wave
   - Amplitude: the *Test Point* value from the *AC Amplitude Accuracy Verification* table
   - Frequency: 50 kHz
   - Load impedance: the *Input Impedance* value from the *AC Amplitude Accuracy Verification* table

   Note These values assume you are using a PXI-5402 function generator. For other function generators, the output voltage varies with load output impedance, up to doubling the voltage for a high impedance load.
5. Wait one second for the output of the function generator to settle.
6. Measure the output voltage amplitude using the PXIe-5162 and the DMM.
7. Record the V RMS measurements.
8. Calculate the amplitude error using the following formula:

   $AC\ Voltage\ Error = 20 \times \log_{10}(V_{\text{PXIe-5162 Measured}} / V_{\text{DMM Measured}})$
9. Compare the amplitude error to the appropriate limit from the *AC Amplitude Accuracy Verification* table
10. Change the maximum input frequency to 175 MHz and repeat steps *5* on page 21 through *9* on page 21.
11. Change the maximum input frequency to 20 MHz and repeat steps *5* on page 21 through *9* on page 21.

    Note If you are calibrating the PXIe-5162 (4 CH), skip step *12* on page 21 for input channels 1 and 3.
12. Configure the device with the following settings and repeat steps *5* on page 21 through 11:
    - Maximum input frequency: (1 MΩ) 300 MHz, (50 Ω) 1,500 MHz
    - Sample clock timebase multiplier: 2
    - Sample clock timebase divisor: 200

13. Configure the device with the following settings and repeat steps *5* on page 21 through 11:
    - Maximum input frequency: (1 MΩ) 300 MHz, (50 Ω) 1,500 MHz
    - Sample clock timebase multiplier: 1
    - Sample clock timebase divisor: 100
14. Repeat steps *2* on page 20 through 13 for each configuration listed in the *AC Amplitude Accuracy Verification* table.
15. Connect the DMM and function generator to channel 1 of the PXIe-5162 as shown in the *AC Verification Test Connections* figure and repeat steps *2* on page 20 through 13 for each configuration listed in the *AC Amplitude Accuracy Verification* table.

    Note If you are verifying the PXIe-5162 (4 CH), proceed to the following steps. If you are verifying the PXIe-5162 (2 CH), AC amplitude accuracy verification is complete.

16. Connect the DMM and function generator to channel 2 of the PXIe-5162 as shown in the *AC Verification Test Connections* figure and repeat steps *2* on page 20 through 13 for each configuration listed in the *AC Amplitude Accuracy Verification* table.
17. Connect the DMM and function generator to channel 3 of the PXIe-5162 as shown in the *AC Verification Test Connections* figure and repeat steps *2* on page 20 through 13 for each configuration listed in the *AC Amplitude Accuracy Verification* table.

Verifying 50 Ω Bandwidth

Follow this procedure to verify the analog bandwidth accuracy of the PXIe-5162 by generating a sine wave and comparing the amplitude measured by the PXIe-5162 to the amplitude measured by the power sensor.

Before performing this procedure, complete the *Test System Characterization* procedure and calculate the *Splitter Balance* of your power splitter.

Table 5. 50 Ω Bandwidth Verification

Config	Vertical Range (V pk-pk)	Test Point		As-Found Limits (dB)	As-Left Limits (dB)
		Frequency (MHz)	Amplitude (dBm)		
1	0.05 V	0.05	-18.5	—	—
2	0.05 V	1,500.1	-18.5	-3.00 to 1.00	-1.62 to 1.00
3	2 V	0.05	13.5	—	—
4	2 V	1,500.1	13.5	-3.00 to 1.00	-1.62 to 1.00

1. Connect splitter output 2 of the power sensor assembly from the *Test System Characterization* section to channel 0 of the PXIe-5162.

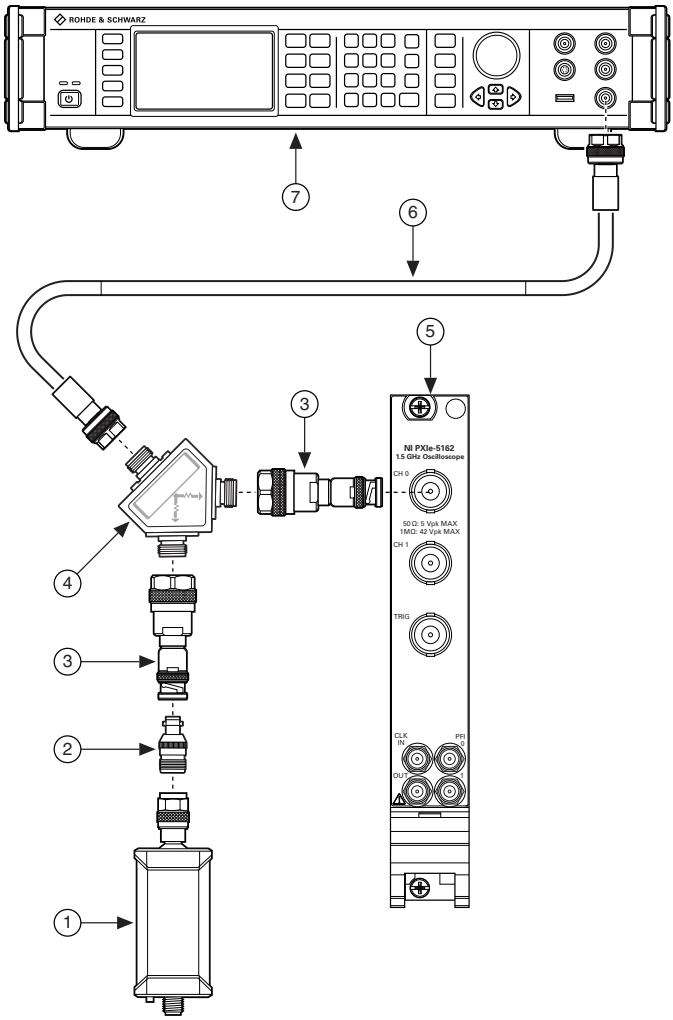
    Note The power sensor assembly must match the configuration used in the *Test System Characterization* section, in which the power sensor is connected to

splitter output 1 and the signal generator is connected to the input port of the power splitter.

The following figure illustrates the hardware setup.

Figure 9. 50 Ω Bandwidth Verification Cabling Diagram

Notice Provide strain relief for connectors on the DUT in order to prevent damage to the instrument.



1. Power sensor
2. BNC (f)-to-N (f) Adapter
3. Type N (m)-to-BNC (m) adapter
4. Keysight 11667A power splitter
5. PXIe-5162
6. Type N (m)-to-Type N (m) cable
7. Signal generator

2. Configure the PXIe-5162 with the following settings:
   - Input impedance: 50 Ω
   - Maximum input frequency: 1,500 MHz
   - Vertical offset: 0 V
   - Vertical range: the Vertical Range value from the *50 Ω Bandwidth Verification* table
   - Minimum number of points: 1,048,576 samples
   - Sample clock timebase source: VAL_INTERNAL_TIMEBASE
   - Sample clock timebase rate: 2.5 GS/s
   - Sample clock timebase multiplier: 1
   - Sample clock timebase divisor:
     – If the *Test Point Frequency* value from the *50 Ω Bandwidth Verification* table is 50 kHz, set this value to 100.
     – For all other *Test Point Frequency* values, set this value to 2.

   Note The actual sample rate of the PXIe-5162 is calculated by the following formula:
   25 MS/s = (*Sample Clock Timebase Rate* × *Sample Clock Timebase Multiplier*) / *Sample Clock Termbase Divisor*
3. Configure the signal generator to generate a sine waveform with the following characteristics into a 50 Ω load:
   - Frequency: the *Test Point Frequency* value from the *50 Ω Bandwidth Verification* table
   - Amplitude level: the *Test Point Amplitude* value from the *50 Ω Bandwidth Verification* table
4. Configure the power sensor to correct for the Test Point Frequency using the power sensor frequency correction function.
5. Use the power sensor to measure the power in dBm.

   Record the result as *Measured Input Power*.
6. Calculate the corrected input power using the following equation:

   Corrected Input Power = Measured Input Power + Splitter Balance

   Note Select the *Splitter Balance* value from the list of test points from the *Test System Characterization* section for the current Test Point Frequency.
7. Use the PXIe-5162 to acquire and measure the power using the Extract Single Tone Information VI, converting the result from V peak to dBm.

   Record the result as *Device Input Power*.
8. If the *Test Point Frequency* value from the *50 Ω Bandwidth Verification* table is 50 kHz, proceed to the following step. Otherwise, go to step *11* on page 25.
9. Calculate the *Power Reference* using the following equation:

   Power Reference = Device Input Power - Corrected Input Power
10. Go to step *13* on page 26. The power error is not calculated for this configuration.
11. Calculate the *Power Error* using the following equation:

Power Error = Device Input Power - Corrected Input Power - Power Reference

12. Compare the power error to the appropriate Limit from the *50 Ω Bandwidth Verification* table.
13. Repeat steps *2* on page 25 through *12* on page 26 for each configuration in the *50 Ω Bandwidth Verification* table.
14. Connect splitter output 2 of the power sensor assembly to channel 1 of the PXIe-5162 and repeat steps *2* on page 25 through *12* on page 26 for each configuration listed in the *50 Ω Bandwidth Verification* table.

Note If you are verifying the PXIe-5162 (4 CH), proceed to the following steps. If you are verifying the PXIe-5162 (2 CH), 50 Ω bandwidth verification is complete.

15. Connect splitter output 2 of the power sensor assembly to channel 2 of the PXIe-5162 and repeat steps *2* on page 25 through *12* on page 26 for each configuration listed in the *50 Ω Bandwidth Verification* table.
16. Connect splitter output 2 of the power sensor assembly to channel 3 of the PXIe-5162 and repeat steps *2* on page 25 through *12* on page 26 for each configuration listed in the *50 Ω Bandwidth Verification* table.

Verifying 1 MΩ Bandwidth

Follow this procedure to verify the 1 MΩ analog bandwidth accuracy of the PXIe-5162 by generating a sine wave and comparing the amplitude measured by the PXIe-5162 to the amplitude measured by the power sensor.

Before performing this procedure, complete the *Test System Characterization* procedure and calculate the *Splitter Balance* of your power splitter.

Table 6. 1 MΩ Bandwidth Verification

Config	Vertical Range (V pk-pk)	Test Point		As-Found Limits (dB)	As-Left Limits (dB)
		Frequency (MHz)	Amplitude (dBm)		
1	1 V	0.05	7.5	—	—
2	1 V	300.1	7.5	-3.00 to 1.00	-2.55 to 1.00
3	2 V	0.05	13.5	—	—
4	2 V	250.1	13.5	-3.00 to 1.00	-2.68 to 1.00
5	10 V	0.05	16	—	—
6	10 V	250.1	16	-3.00 to 1.00	-2.68 to 1.00

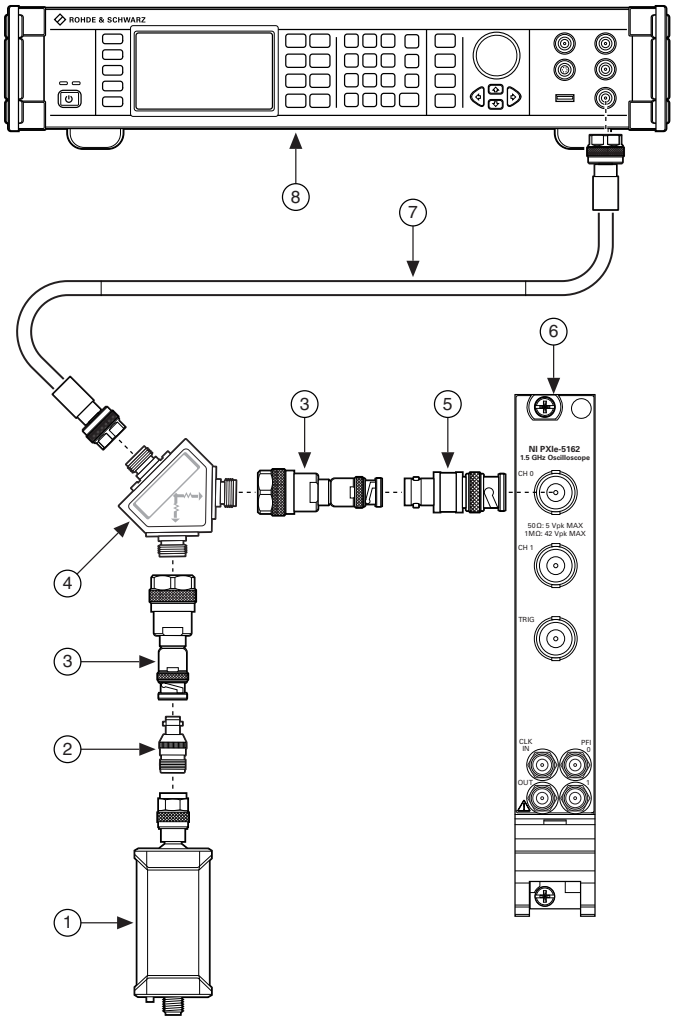
1. Connect the 50 Ω BNC feed-through terminator to channel 0 of the PXIe-5162. Connect splitter output 2 of the power sensor assembly from the *Test System Characterization* section to the 50 Ω BNC feed-through terminator.

   Note The power sensor assembly must match the configuration used in the *Test System Characterization* section, in which the power sensor is connected to splitter output 1 and the signal generator is connected to the input port of the power splitter.

   The following figure illustrates the hardware setup.

Figure 10. 1 MΩ Bandwidth Verification Cabling Diagram

Notice Provide strain relief for connectors on the DUT in order to prevent damage to the instrument.



1. Power sensor
2. BNC (f)-to-N (f) Adapter
3. Type N (m)-to-BNC (m) adapter
4. Keysight 11667A power splitter
5. 50 Ω BNC feed-thru terminator
6. PXIe-5162
7. Type N (m)-to-Type N (m) cable
8. Signal generator

2. Configure the PXIe-5162 with the following settings:
   - Input impedance: 1 MΩ
   - Maximum input frequency: 300 MHz
   - Vertical offset: 0 V
   - Vertical range: the *Vertical Range* value from the *1 MΩ Bandwidth Verification* table
   - Minimum number of points: 1,048,576 samples
   - Sample clock timebase source: VAL_INTERNAL_TIMEBASE
   - Sample clock timebase rate: 2.5 GS/s
   - Sample clock timebase multiplier: 1
   - Sample clock timebase divisor:
     – If the *Test Point Frequency* value from the *1 MΩ Bandwidth Verification* table is 50 kHz, set this value to 100.
     – For all other *Test Point Frequency* values, set this value to 2.

   Note The actual sample rate of the PXIe-5162 is calculated by the following formula:
   25 MS/s = (*Sample Clock Timebase Rate* × *Sample Clock Timebase Multiplier*) / *Sample Clock Timebase Divisor*
3. Configure the signal generator to generate a sine waveform with the following characteristics:
   - Frequency: the *Test Point Frequency* value from the *1 MΩ Bandwidth Verification* table
   - Amplitude level: the *Test Point Amplitude* value from the *1 MΩ Bandwidth Verification* table
4. Configure the power sensor to correct for the *Test Point Frequency* using the power sensor frequency correction function.
5. Use the power sensor to measure the power in dBm.

   Record the result as *Measured Input Power*.
6. Calculate the corrected input power using the following equation:

   Corrected Input Power = Measured Input Power + Splitter Balance

   Note Select the *Splitter Balance* value from the list of test points from the *Test System Characterization* section for the current Test Point Frequency.
7. Use the PXIe-5162 to acquire and measure the power using the Extract Single Tone Information VI, converting the result from V peak to dBm.

   Record the result as *Device Input Power*.
8. If the Test Point Frequency value from the *1 MΩ Bandwidth Verification* table is 50 kHz, proceed to the following step. Otherwise, go to step *11* on page 29.
9. Calculate the *Power Reference* using the following equation:

   Power Reference = Device Input Power - Corrected Input Power
10. Go to step *13* on page 30. The power error is not calculated for this configuration.
11. Calculate the *Power Error* using the following equation:

Power Error = Device Input Power - Corrected Input Power - Power Reference

12. Compare the power error to the appropriate Limit from the *1 MΩ Bandwidth Verification* table.
13. Repeat steps *2* on page 29 through *12* on page 30 for each configuration in the *1 MΩ Bandwidth Verification* table.
14. Connect the 50 Ω BNC feed-through terminator to channel 1 of the PXIe-5162. Connect splitter output 2 of the power sensor assembly to the 50 Ω BNC feed-through terminator and repeat steps *2* on page 29 through *12* on page 30 for each configuration in the *1 MΩ Bandwidth Verification* table.

Note If you are verifying the PXIe-5162 (4 CH), proceed to the following steps. If you are verifying the PXIe-5162 (2 CH), 1 MΩ bandwidth verification is complete.

15. Connect the 50 Ω BNC feed-through terminator to channel 2 of the PXIe-5162. Connect splitter output 2 of the power sensor assembly to the 50 Ω BNC feed-through terminator and repeat steps *2* on page 29 through *12* on page 30 for each configuration in the *1 MΩ Bandwidth Verification* table.
16. Connect the 50 Ω BNC feed-through terminator to channel 3 of the PXIe-5162. Connect splitter output 2 of the power sensor assembly to the 50 Ω BNC feed-through terminator and repeat steps *2* on page 29 through *12* on page 30 for each configuration in the *1 MΩ Bandwidth Verification* table.

Verifying Timebase Accuracy

Follow this procedure to verify the frequency accuracy of the PXIe-5162 onboard timebase using an oscilloscope calibrator.

Table 7. Timebase Accuracy Verification

As-Found Limit	As-Left Limit
±25 ppm (±2,500 Hz)	±24.42 ppm (±2,442 Hz)

1. Connect the calibrator test head to channel 0 of the PXIe-5162.
2. Configure the PXIe-5162 with the following settings:
   - Input impedance: 50 Ω
   - Maximum input frequency: 1,500 MHz
   - Vertical range (V pk-pk): 1 V
   - Sample rate: 1.25 GS/s
   - Minimum number of points: 1,048,576 samples
3. Configure the calibrator and generate a waveform with the following characteristics:
   - Waveform: Sine wave
   - Amplitude (V pk-pk): 0.9 V
   - Frequency: 100 MHz
   - Load impedance: 50 Ω
4. Enable the calibrator output.

5. Wait one second for settling, then measure and record the peak frequency using the Extract Single Tone Information VI.

   Record the result as $F_{Measured}$.
6. Calculate the timebase error using the following formula:

   $Timebase\ Error = (F_{Measured} - (100 \times 10^6)) / 100$ [ppm]
7. Compare the timebase error to the appropriate limit from the *Timebase Accuracy Verification* table.

   Note Timebase verification is required on only one channel.
8. Disable the calibrator output.

Verifying Input Impedance

Follow this procedure to verify the input impedance of the PXIe-5162 using an oscilloscope calibrator.

Table 8. Input Impedance Verification

Config	Vertical Range (V pk-pk)	Input Impedance (Ω)	As-Found Test Limits (Ω)	As-Left Test Limits (Ω)
1	1 V	50	±0.875	±0.48
2	2 V	50	±0.875	±0.48
3	1 V	1 M	±9000	±7000
4	10 V	1 M	±9000	±7000
5	20 V	1 M	±9000	±7000

1. Connect the calibrator test head to channel 0 of the PXIe-5162.
2. Configure the PXIe-5162 with the following settings:
   - Input impedance: the Input Impedance value from the *Input Impedance Verification* table.
   - Maximum input frequency: (50 Ω) 500 MHz, (1 MΩ), 300 MHz
   - Vertical offset: 0 V
   - Vertical range: the Vertical Rage value from the *Input Impedance Verification* table.
   - Sample rate: 2.5 GS/s
   - Minimum number of points: 50,000 samples
3. Configure the calibrator output impedance to match that of the PXIe-5162.
4. Configure the calibrator to measure impedance.
5. Enable the calibrator.
6. Wait one second for settling, then record the measured impedance.
7. Use the following formula to calculate the input impedance error:

Input Impedance Error = $Impedance_{Measured}$ - *Input Impedance* from the *Input Impedance Verification* table

8. Compare the input impedance error to the appropriate limit from the *Input Impedance Verification* table.
9. Repeat steps *2* on page 31 through *8* on page 32 for each configuration listed in the *Input Impedance Verification* table.
10. Connect the calibrator test head to channel 1 of the PXIe-5162 and repeat steps *2* on page 31 through *8* on page 32 for each configuration listed in the *Input Impedance Verification* table.

Note If you are verifying the PXIe-5162 (4 CH), proceed to the following steps. If you are verifying the PXIe-5162 (2 CH), input impedance verification is complete.

11. Connect the calibrator test head to channel 2 of the PXIe-5162 and repeat steps *2* on page 31 through *8* on page 32 for each configuration listed in the *Input Impedance Verification* table.
12. Connect the calibrator test head to channel 3 of the PXIe-5162 and repeat steps *2* on page 31 through *8* on page 32 for each configuration listed in the *Input Impedance Verification* table.

Verifying Input Capacitance

Follow this procedure to verify in the input capacitance of the PXIe-5162 using an oscilloscope calibrator.

Table 9. Input Capacitance Verification

Config	Vertical Range (V pk-pk)	As-Found Test Limits (pF)	As-Left Test Limits (pF)
0	1 V	12.5 to 17.5	12.9 to 17.1
1	10 V	12.5 to 17.5	12.9 to 17.1
2	20 V	12.5 to 17.5	12.9 to 17.1

1. Connect the calibrator test head to channel 0 of the PXIe-5162.
2. Configure the PXIe-5162 with the following settings:
   - Input impedance: 1 MΩ
   - Maximum input frequency: 300 MHz
   - Vertical offset: 0 V
   - Vertical range: the *Vertical Range* value from the *Input Capacitance Verification* table
   - Sample rate: 2.5 GS/s
   - Minimum number of points: 50,000 samples
3. Configure the calibrator to measure capacitance.
4. Enable the calibrator.
5. Wait one second for settling, then record the measured capacitance.

6. Compare the measured capacitance to the appropriate limit from the *Input Capacitance Verification* table.
7. Repeat steps *2* on page 32 through *6* on page 33 for each configuration listed in the *Input Capacitance Verification* table.
8. Connect the calibrator test head to channel 1 of the PXIe-5162 and repeat steps *2* on page 32 through *6* on page 33 for each configuration listed in the *Input Capacitance Verification* table.

Note If you are verifying the PXIe-5162 (4 CH), proceed to the following steps. If you are verifying the PXIe-5162 (2 CH), input capacitance verification is complete.

9. Connect the calibrator test head to channel 2 of the PXIe-5162 and repeat steps *2* on page 32 through *6* on page 33 for each configuration listed in the *Input Capacitance Verification* table.
10. Connect the calibrator test head to channel 3 of the PXIe-5162 and repeat steps *2* on page 32 through *6* on page 33 for each configuration listed in the *Input Capacitance Verification* table.

Verifying RMS Noise

Follow this procedure to verify the RMS noise of the PXIe-5162 using a 50 Ω terminator.

Table 10. RMS Noise Verification

Config	Input Impedance (Ω)	Vertical Range (V pk-pk)	Max Input Frequency (MHz)	As-Found Test Limit (% of FS)	As-Left Test Limit (% of FS)
1	50	0.05 V	20	0.62	0.55
2	50	1 V	20	0.34	0.28
3	50	0.05 V	175	0.62	0.55
4	50	1 V	175	0.34	0.28
5	50	0.05 V	1,500	0.62	0.55
6	50	0.1 V	1,500	0.39	0.33
7	50	0.2 V	1,500	0.34	0.28
8	50	0.5 V	1,500	0.34	0.28
9	50	1 V	1,500	0.34	0.28
10	50	2 V	1,500	0.34	0.28
11	50	5 V	1,500	0.34	0.28
12	1 M	0.05 V	20	0.62	0.55

Table 10. RMS Noise Verification (Continued)

Config	Input Impedance (Ω)	Vertical Range (V pk-pk)	Max Input Frequency (MHz)	As-Found Test Limit (% of FS)	As-Left Test Limit (% of FS)
13	1 M	1 V	20	0.34	0.28
14	1 M	0.05 V	175	0.62	0.55
15	1 M	1 V	175	0.34	0.28
16	1 M	0.05 V	300	0.62	0.55
17	1 M	0.1 V	300	0.39	0.33
18	1 M	0.2 V	300	0.34	0.28
19	1 M	0.5 V	300	0.34	0.28
20	1 M	1 V	300	0.34	0.28
21	1 M	2 V	300	0.34	0.28
22	1 M	5 V	300	0.34	0.28
23	1 M	10 V	300	0.34	0.28
24	1 M	20 V	300	0.34	0.28
25	1 M	50 V	300	0.34	0.28

1. Connect the 50 Ω terminator to channel 0 of the PXIe-5162.
2. Configure the PXIe-5162 with the following settings:
   - Input impedance: the Input Impedance value from the *RMS Noise Verification* table
   - Maximum input frequency: the Max Input Frequency value from the *RMS Noise Verification* table
   - Vertical offset: 0 V
   - Vertical range: the Vertical Range value from the *RMS Noise Verification* table
   - Sample rate: 2.5 GS/s
   - Minimum number of points: 1,048,576 samples
3. Use the PXIe-5162 to acquire a waveform, then calculate the standard deviation of the acquired waveform. Use the standard deviation to compute the RMS noise using the following formula:

   RMS Noise (% of FS) = (100 × σ) / *Vertical Range*
   where σ is the standard deviation of the acquired waveform.
4. Compare the RMS noise to the appropriate Limit from the *RMS Noise Verification* table.
5. Repeat steps *2* on page 34 through *4* on page 34 for each configuration listed in the *RMS Noise Verification* table.

6. Connect the 50 Ω terminator to channel 1 of the PXIe-5162 and repeat steps *2* on page 34 through *4* on page 34 for each configuration listed in the *RMS Noise Verification* table.

Note If you are verifying the PXIe-5162 (4 CH), proceed to the following steps. If you are verifying the PXIe-5162 (2 CH), RMS noise verification is complete.

7. Connect the 50 Ω terminator to channel 2 of the PXIe-5162 and repeat steps *2* on page 34 through *4* on page 34 for each configuration listed in the *RMS Noise Verification* table.
8. Connect the 50 Ω terminator to channel 3 of the PXIe-5162 and repeat steps *2* on page 34 through *4* on page 34 for each configuration listed in the *RMS Noise Verification* table.

Adjustment

Follow this procedure to externally adjust the PXIe-5162.

Table 11. Vertical Range Adjustment

Config	Input Impedance (Ω)	Vertical Range (V pk-pk)	Input (V)
1	1 M	50 V	22.500
2	1 M	50 V	-22.500
3	1 M	20 V	9.000
4	1 M	20 V	-9.000
5	1 M	10 V	4.500
6	1 M	10 V	-4.500
7	1 M	5 V	2.250
8	1 M	5 V	-2.250
9	1 M	2 V	0.900
10	1 M	2 V	-0.900
11	1 M	1 V	0.450
12	1 M	1 V	-0.450
13	1 M	0.631 V	0.284
14	1 M	0.631 V	-0.284
15	1 M	0.5 V	0.225
16	1 M	0.5 V	-0.225
17	1 M	0.2 V	0.090

Table 11. Vertical Range Adjustment (Continued)

Config	Input Impedance (Ω)	Vertical Range (V pk-pk)	Input (V)
18	1 M	0.2 V	-0.090
19	1 M	0.1 V	0.045
20	1 M	0.1 V	-0.045
21	1 M	0.05 V	0.023
22	1 M	0.05 V	-0.023
23	50	0.05 V	0.023
24	50	0.05 V	-0.023
25	50	0.1 V	0.045
26	50	0.1 V	-0.045
27	50	0.2 V	0.090
28	50	0.2 V	-0.090
29	50	0.5 V	0.225
30	50	0.5 V	-0.225
31	50	0.631 V	0.284
32	50	0.631 V	-0.284
33	50	1 V	0.450
34	50	1 V	-0.450
35	50	2 V	0.900
36	50	2 V	-0.900
37	50	5 V	2.250
38	50	5 V	-2.250

Table 12. 1 MΩ Compensation Attenuator Adjustment

Config	Input Impedance (Ω)	Vertical Range (V pk-pk)	Input (V)
1	1 M	1 V	0.500
2	1 M	1 V	0.900

Table 12. 1 MΩ Compensation Attenuator Adjustment (Continued)

Config	Input Impedance (Ω)	Vertical Range (V pk-pk)	Input (V)
3	1 M	10 V	5.000
4	1 M	10 V	9.000
5	1 M	50 V	25.000
6	1 M	50 V	45.000

Table 13. External Trigger Range Adjustment

Config	Input Impedance (Ω)	Vertical Range (V pk-pk)	Input (V)
1	1 M	10 V	4.500
2	1 M	10 V	-4.500
3	1 M	1 V	0.450
4	1 M	1 V	-0.450
5	50	5 V	2.250
6	50	5 V	-2.250

1. Call the niScope Cal Start VI to obtain an NI-SCOPE external calibration session.
2. Connect the calibrator test head to channel 0 of the PXIe-5162.
3. Configure the calibrator output impedance to the *Input Impedance* value from the *Vertical Range Adjustment* table.
4. Configure the calibrator output voltage to the DC *Input* value from the *Vertical Range Adjustment* table.
5. Enable the calibrator output.
6. Wait one second for settling.
7. Call the niScope Cal Adjust Range VI with the following settings to adjust the vertical range:
   - **range**: the *Vertical Range* value from the *Vertical Range Adjustment* table
   - **stimulus**: the *Input* value from the *Vertical Range Adjustment* table
8. Repeat steps *3* on page 37 through *7* on page 37 for each configuration listed in the *Vertical Range Adjustment* table.
9. Disable the calibrator output.
10. Configure the calibrator output impedance to the *Input Impedance* value from the *1 MΩ Compensation Attenuator Adjustment* table.
11. Configure the calibrator to output a 500 Hz symmetrical-to-ground square wave with amplitude equal to the *Input* value from the *1 MΩ Compensation Attenuator Adjustment* table.

12. Enable the calibrator output.
13. Wait one second for settling.
14. Call the niScope Cal Adjust Compensation VI with the following setting to adjust the 1 MΩ compensation attenuator:
    - **range**: the *Vertical Range* value from the *1 MΩ Compensation Attenuator Adjustment* table
15. Repeat steps *10* on page 37 through *14* on page 38 for each configuration listed in the *1 MΩ Compensation Attenuator Adjustment* table.
16. Connect the calibrator test head to channel 1 of the PXIe-5162 and repeat steps *3* on page 37 through *15* on page 38, changing the value of the **channels** parameter from 0 to 1.

    Note If you are adjusting the PXIe-5162 (4 CH), proceed to the following steps. If you are adjusting the PXIe-5162 (2 CH), go to step *19* on page 38.
17. Connect the calibrator test head to channel 2 of the PXIe-5162 and repeat steps *3* on page 37 through *15* on page 38, changing the value of the **channels** parameter from 0 to 2.
18. Connect the calibrator test head to channel 3 of the PXIe-5162 and repeat steps *3* on page 37 through *15* on page 38, changing the value of the **channels** parameter from 0 to 3.

    Note If you are adjusting the PXIe-5162 (4 CH), go to step *33* on page 39. If you are adjusting the PXIe-5162 (2 CH), proceed to the following steps.
19. Connect the calibrator test head to the external trigger input of the PXIe-5162.
20. Configure the calibrator output impedance to the *Input Impedance* value from the *External Trigger Range Adjustment* table.
21. Configure the calibrator output voltage to the DC *Input* value from the *External Trigger Range Adjustment* table.
22. Enable the calibrator output.
23. Wait one second for settling.
24. Call the niScope Cal Adjust Range VI with the following settings to adjust the vertical range:
    - **channelName**: `VAL_EXTERNAL`
    - **range**: the *Vertical Range* value from the *External Trigger Range Adjustment* table
    - **stimulus**: the *Input* value from the *External Trigger Range Adjustment* table
25. Repeat steps *20* on page 38 through *24* on page 38 for each configuration listed in the *External Trigger Range Adjustment* table.
26. Disable the calibrator output.
27. Configure the calibrator output impedance to the Input Impedance value from the *1 MΩ Compensation Attenuator Adjustment* table.
28. Configure the calibrator to output a 500 Hz symmetrical-to-ground square wave with amplitude equal to the Input value from the *1 MΩ Compensation Attenuator Adjustment* table.

29. Enable the calibrator output.
30. Wait one second for settling.
31. Call the niScope Cal Adjust Compensation Attenuator VI with the following settings to adjust the 1 MΩ compensation attenuator:
    - **channelName**: `VAL_EXTERNAL`
    - **range**: the *Vertical Range* value from the *1 MΩ Compensation Attenuator Adjustment* table
32. Repeat steps *27* on page 38 through *31* on page 39 for each configuration listed in the *1 MΩ Compensation Attenuator Adjustment* table.
33. Disconnect or disable all inputs to the PXIe-5162.
34. Call the niScope Cal Adjust VI with the following settings to adjust the 1 MΩ offset range:
    - **range**: `0`
    - **stimulus**: `0`
35. Call the niScope Cal End VI to close the external calibration session and save the calibration date and temperature.
36. Call the niScope Initialize VI to obtain an NI-SCOPE session.
37. Self-calibrate the PXIe-5162 using the niScope Cal Self Calibrate VI.

Reverification

Repeat the *Verification* section to determine the as-left status of the PXIe-5162.

Note If any test fails reverification after performing an adjustment, verify that you have met the test conditions before returning your PXIe-5162 to NI. Refer to the *Worldwide Support and Services* section for information about support resources or service requests.

Revision History

Part Number	Edition Date	Section	Changes
373910F-01	June 2021	Test Equipment	Added new recommended equipment: • Keysight 11667A power splitter and associated adapters • Rohde & Schwarz NRP18A(N) and NRP6A power sensors • PXI-4071 and PXIe-4081 DMMs • PXI-5406 function generator • Rohde & Schwarz SMA100B signal generator
		Measurement Uncertainty	Removed section
		Verification	Removed measurement uncertainty values

NI Services

Visit *ni.com/support* to find support resources including documentation, downloads, and troubleshooting and application development self-help such as tutorials and examples.

Visit *ni.com/services* to learn about NI service offerings such as calibration options, repair, and replacement.

Visit *ni.com/register* to register your NI product. Product registration facilitates technical support and ensures that you receive important information updates from NI.

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