USER MANUAL

PXIe-6674

PXI Express Timing and Synchronization Module

The PXIe-6674 timing and synchronization module enables you to pass PXI timing and trigger signals between PXI Express chassis without using the chassis' system timing slot. The PXIe-6674 can generate and route clock signals between devices in multiple chassis, providing a method to synchronize multiple devices in a multichassis PXI Express system.

This manual describes the electrical and mechanical aspects of the PXIe-6674 and contains information concerning its operation and programming.

National Instruments Documentation

The PXIe-6674 User Manual is one piece of the documentation set for your measurement system. You could have any of several other documents describing your hardware and software. Use the documentation you have as follows:

- Measurement hardware documentation—This documentation contains detailed information about the measurement hardware that plugs into or is connected to the computer. Use this documentation for hardware installation and configuration instructions, specifications about the measurement hardware, and application hints.
- Software documentation—Refer to the NI-Sync Help, available at *ni.com/manuals*.

You can download NI documentation from *ni.com/manuals*.

Related Documentation

The following documents contain information that you might find helpful as you read this manual:

- *PICMG 2.0 R3.0, CompactPCI Core Specification*, available from PICMG at *www.picmg.org*.
- *PXI Specification, Revision 2.1*, available from *www.pxisa.org*.
- *NI-VISA User Manual*, available form *ni.com/manuals*.
- *NI-VISA Help*, included with the NI-VISA software.
- *NI-Sync User Manual*, available from *ni.com/manuals*.

Contents

NATIONAL INSTRUMENTS

Introduction

The PXIe-6674 timing and synchronization module enables you to share clocks and triggers between modules in a PXI Express chassis and other PXI chassis or non-PXI systems. This is done without using the system timing slot in your PXI Express chassis. The PXIe-6674 module generates and routes clock signals between devices in multiples chassis, providing a method for synchronizing multiple devices in a PXI Express system.

What You Need to Get Started

To set up and use the PXIe-6674, you need the following items:

- PXIe-6674 Timing and Synchronization Module
- PXIe-6674 User Manual
- NI-Sync software.
- One of the following software packages and documentation:
  - LabVIEW
  - LabWindows™/CVI™
  - Microsoft Visual C++ (MSVC)
- PXI EMC filler panels, National Instruments part number 778700-01
- PXI Express chassis
- PXI Express embedded controller or a desktop computer connected to the PXI Express chassis using MXI-Express hardware.

Unpacking

The PXIe-6674 is shipped in an antistatic package to prevent electrostatic damage to the module. Electrostatic discharge (ESD) can damage the module.

Caution Never touch the exposed pins of connectors.

To avoid such damage in handling the module, take the following precautions:

- Ground yourself using a grounding strap or by touching a grounded object.
- Touch the antistatic package to a metal part of the computer chassis before removing the module from the package.

Remove the module from the package and inspect the module for loose components or any sign of damage. Notify NI if the module appears damaged in any way. Do not install a damaged module into the computer.

Store the PXIe-6674 in the antistatic envelope when not in use.

Software Programming Choices

When programming the PXIe-6674, you can use NI application development environment (ADE) software such as LabVIEW or LabWindows/CVI, or you can use other ADEs such as Visual C/C++.

LabVIEW features interactive graphics, a state-of-the-art interface, and a powerful graphical programming language. The LabVIEW Data Acquisition VI Library, a series of virtual instruments for using LabVIEW with National Instruments DAQ hardware, is included with LabVIEW.

LabWindows/CVI is a complete ANSI C ADE that features an interactive user interface, code generation tools, and the LabWindows/CVI Data Acquisition and Easy I/O libraries.

Safety Information

The following section contains important safety information that you must follow when installing and using the product.

Do not operate the product in a manner not specified in this document. Misuse of the product can result in a hazard. You can compromise the safety protection built into the product if the product is damaged in any way. If the product is damaged, return it to National Instruments for repair.

Do not substitute parts or modify the product except as described in this document. Use the product only with the chassis, modules, accessories, and cables specified in the installation instructions. You must have all covers and filler panels installed during operation of the product.

Do not operate the product in an explosive atmosphere or where there maybe flammable gases or fumes. If you must operate the product in such an environment, it must be in a suitably rated enclosure.

If you need to clean the product, use a soft, nonmetallic brush. The product must be completely dry and free from contaminants before you return it to service.

Operate the product only at or below Pollution Degree 2. Pollution is foreign matter in a solid, liquid, or gaseous state that can reduce dielectric strength or surface resistivity. The following is a description of pollution degrees.

- Pollution Degree 1 means no pollution or only dry, nonconductive pollution occurs. The pollution has no influence.
- Pollution Degree 2 means that only nonconductive pollution occurs in most cases. Occasionally, however, a temporary conductivity caused by condensation must be expected.
- Pollution Degree 3 means that conductive pollution occurs, or dry, nonconductive pollution occurs that becomes conductive due to condensation.

You must initiate signal connections for the maximum voltage for which the product is rated. Do no exceed the maximum ratings for the product. Do not install wiring while the product is live with electrical signals. Do not remove or add connector blocks when power is connected to the system. Avoid contact between your body and the connector block signal when hot swapping modules. Remove power from signal lines before connecting them to or disconnecting them from the product.

Operate the product at or below the measurement category[1] marked on the hardware label. Measurement circuits are subjected to working voltages[2] and transient stresses (overvoltage) from the circuit to which they are connected during measurement or test. Measurement categories establish standard impulse withstand voltage levels that commonly occur in electrical distribution systems. The following is a description of measurement categories:

- Measurement Category I is for measurements performed on circuits not directly connected to the electrical distribution system referred to as MAINS voltage. This category is for measurements of voltages from specially protected secondary circuits. Such voltage measurements include signal levels, special hardware, and limited-energy parts of hardware, circuits powered by regulated low-voltage sources, and electronics.
- Measurement Category II is for measurements performed on circuits directly connected to the electrical distribution system (MAINS[3]). This category refers to local-level electrical distribution, such as that provided by a standard wall outlet (for example, 115 AC voltage for U.S. or 230 AC voltage for Europe). Examples of Measurement Category II are measurements performed on household appliances, portable tools, and similar hardware.
- Measurement Category III is for measurements performed in the building installation at the distribution level. This category refers to measurements on hard-wired hardware such as hardware in fixed installations, distribution boards, and circuit breakers. Other examples are wiring, including cables, bus bars, junction boxes, switches, socket outlets

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[1] Measurement categories, also referred to as overvoltage or installation categories, are defined in electrical safety standard IEC 61010-1 and IEC 60664-1.

[2] Working voltage is the highest rms value of an AC or DC voltage that can occur across any particular insulation.

[3] MAINS is defined as a hazardous live electrical supply system that powers hardware. Suitably rated measuring circuits may be connected to the MAINS for measuring purposes.

in the fixed installation, and stationary motors with permanent connections to fixed installations.

- Measurement Category IV is for measurements performed at the primary electrical supply installation, typically outside buildings. Examples include electricity meters and measurements on primary overcurrent protection devices and on ripple control units.

Installing and Configuring

This chapter describes how to install the PXIe-6674 hardware and software and how to configure the device.

Installing the Software

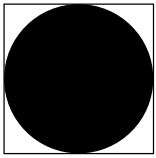
Refer to the `readme.htm` file that accompanies the NI-Sync software for software installation directions.

Installing the Hardware

The following are general installation instructions. Consult the chassis user manual or technical reference manual for specific instructions and warnings about installing new modules.

1. Power off and unplug the chassis.
2. Locate the desired slot in your PXI Express chassis. The PXIe-6674 can be placed in any PXI Express slot, as indicated by the glyph in *Figure 1.* on page 5

Figure 1. PXI Express Slot Indicator Glyph



3. Remove the filler panel for the selected slot, if applicable.
4. Ground yourself using a grounding strap or by touching a grounded object. Follow the ESD protection precautions described in the *Unpacking* section of the *Introduction*.
5. Carefully insert the PXIe-6674 into the slot, making sure to not scrape the module on any adjacent modules. Use the injector/ejector handle to fully insert the module into the chassis.
6. Screw the front panel of the device to the front panel mounting rail of the chassis.
7. If adjacent slots are not populated, use EMC filler panels to cover the opening.

Caution To ensure the specified EMC performance, you must install PXI EMC filler panels, National Instruments part number 778700-01, in all open chassis slots.

8. Visually verify the installation. Ensure that the module is fully inserted into the slot.
9. Plug in and power on the chassis.

The PXIe-6674 is now installed.

Configuring the Module

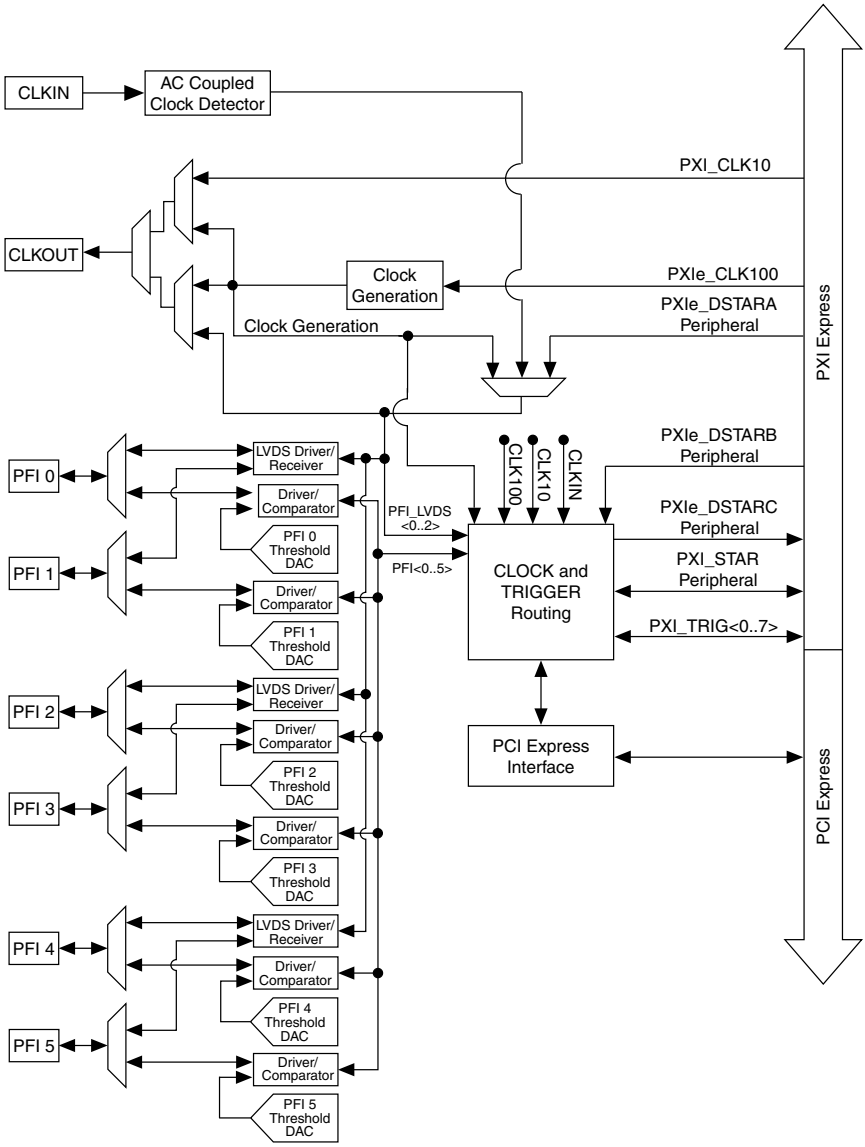
The PXIe-6674 is completely software configurable. The system software automatically allocates all module resources.

The two LEDs on the front panel provide information about module status. The front panel descriptions in the Hardware Overview describe the LEDs in greater detail.

Hardware Overview

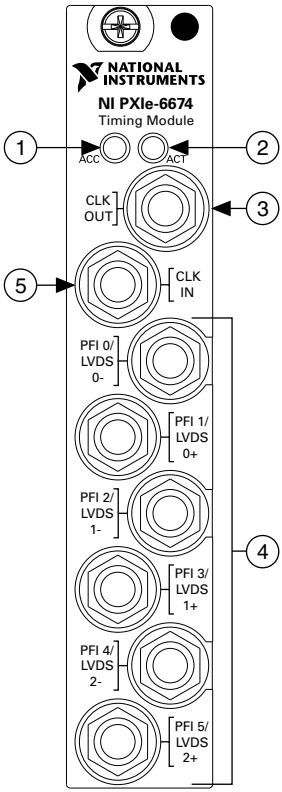
This chapter presents an overview of the hardware functions of the PXIe-6674. *Figure 2.* on page 7 provides a functional overview of the PXIe-6674 hardware.

Figure 2. Functional Overview of the PXIe-6674



PXIe-6674 Front Panel and LED

Figure 3. PXIe-6674 Front Panel



1. Access LED
2. Active LED
3. CLKOUT Connector
4. PFI<0..5>/PFI_LVDS<0..2> Connectors
5. CLKIN Connector

Table 1. Signal Descriptions

Signal	Description
CLKIN	AC coupled, 50 Ω clock input. CLKIN can be routed to the FPGA for use as a synchronization clock.
CLKOUT	AC coupled clock output. CLKOUT can be sourced from the PXI-CLK10, Clock Generation, or from the PXIe_DSTARA line.
PFI or PFI_LVDS	Programmable Function Interface which can be individually configured for either single ended operation or LVDS operation. In LVDS mode, the connectors are paired and can be programmatically set as either inputs or outputs, but not both simultaneously.

Caution Connections that exceed any of the maximum ratings of input or output signals on the PXIe-6674 can damage the module and the computer. NI is not liable for any damage resulting from such signal connections.

Table 2. Access LED

Color	Status
Off	Module is not yet functional.
Green	Driver has initiated the module.
Amber	Module is being accessed. The Access LED flashes amber for 50 ms when the module is accessed.
Blinking Red	Module has detected an over-temperature condition.
Solid Red	A hardware error has been detected.

Caution If the Access LED is observed to be blinking red, the module has detected an over-temperature condition. Continued use of the PXIe-6674 in this condition is not recommended as product reliability may become compromised. Since several common problems can cause an over-temperature condition, please investigate the following:

- Check that all chassis covers, filler panels, and/or slot blockers are installed.
- Make sure that the chassis fan speed is set to the highest setting.
- If applicable, check that the chassis fan air intake is not blocked and that the fan filters are clean.
- Make sure that the ambient temperature around the chassis isn't above the rated temperature specifications. If so, move the chassis to a cooler ambient temperature location.

Caution If the Access LED is observed to be solid red, a hardware failure has been detected that may impact the performance of the PXIe-6674. Contact National Instruments for support.

Active LED

You can set the Active LED to amber.

Tip Changing the Active LED color to amber is helpful when you want to identify devices in a multichassis situation, or when you want an indication that your application has reached a predetermined section of the code.

Hardware Features

The PXIe-6674 performs two broad functions.

- Generating clock and trigger signals.
- Routing internally or externally generated signals from one location to another.

Table 3. on page 10 outlines the function and direction of the signals discussed in detail in the remainder of this chapter.

Table 3. Signal Descriptions

Signal Name	Direction	Description
PXI_CLK10	In (from chassis)	This signal is the PXI 10 MHz backplane clock. This signal is the output of the native 100 MHz oscillator in the chassis divided by ten.
PXIe_CLK100	In (from chassis)	This signal is the PXI Express 100 MHz backplane clock. PXIe-CLK100 offers tighter slot to slot timing than PXI_CLK10.
CLKIN	In (from front panel)	CLKIN is the signal connected to the SMA input connector of the same name. CLKIN is connected to the FPGA for use as a synchronization clock.
CLKOUT	Out (to front panel)	CLKOUT is the signal on the SMA output connector of the same name. CLKOUT can be sourced from the OCXO, PXI_CLK10, Clock Generation, or from the PXIe_DSTARA network.
Clock Generation	Out (internal)	Clock Generation refers to the clock signal coming from the onboard clock generation circuitry of the PXIe-6674. The clock generation circuitry can generate a clock from sub-1 Hz to 1 GHz with fine granularity and is automatically locked in phase to PXIe_CLK100.

Table 3. Signal Descriptions (Continued)

Signal Name	Direction	Description
PFI<0..5>	In/Out (to/ from front panel)	The single ended Programmable Function Interface (PFI) pins on the PXIe-6674 route timing and triggering signals between multiple PXI Express chassis. A wide variety of input and output signals can be routed to or from the PFI lines.
PFI_LVDS<0..2>	In/Out (to/ from front panel)	The LVDS Programmable Function Interface can be used to route timing and triggering signals between multiple PXI Express chassis. The use of LVDS logic allows much faster speeds than can be achieved with the single ended PFIs. The LVDS PFIs, when used as outputs, can be sourced from the PXIe_DSTARA network, the FPGA, or the clock generation circuitry. As inputs, the LVDS PFIs can be routed to the PXIe_DSTARA network and to the FPGA.
PXI_TRIG<0..7>	In/Out (to/ from chassis)	The PXI trigger bus consists of eight digital lines shared among all slots in the PXI Express chassis. The PXIe-6674 can route a wide variety of signals to and from these lines.  **Note** PXI_TRIG<0..5> are also known as RTSI<0..5> in some hardware devices and APIs. However, PXI_TRIG<6..7> are not identical to RTSI<6..7>.
PXI_STAR	In/Out (to/ from chassis)	The PXI star trigger bus connects the system timing slot to other peripheral slots in a star configuration. The electrical paths of each star line are closely matched to minimize intermodule skew. The PXIe-6674 connects to the PXI_STAR line for the slot the device is located in.
PXIe_DSTARA	In (from chassis)	The PXIe-DSTARA lines connect the system timing module to each peripheral slot in a PXI Express chassis, allowing the system timing module to distribute a clock signal to every slot. PXIe-DSTARA uses differential LVPECL signaling and is capable of high speed clock distribution.

Table 3. Signal Descriptions (Continued)

Signal Name	Direction	Description
PXIe_STARB	In (from chassis)	The PXIe_DSTARB lines connect the system timing module to each peripheral slot in a PXI Express chassis, allowing the system timing module to send out high speed triggers to every slot. PXI_DSTARB uses differential LVDS signaling and is capable of sending out higher speed trigger signals.
PXIe_DSTARC	Out (to chassis)	The PXIe_DSTARC lines connect each peripheral slot in a PXI Express chassis to the system timing module, allowing the system timing module to receive high speed clock and trigger signals from every slot. PXIe_DSTARC uses differential LVDS signaling.

The remainder of this chapter describes how these signals are used, acquired, and generated by the PXIe-6674 hardware, and explains how you can route the signals between various locations to synchronize multiple measurement devices and PXI chassis.

Generating and Routing Clocks

The PXIe-6674 can generate a clock using the onboard clock generation circuitry. The following section describes the clock generation functionality and resources available on the PXIe-6674 for routing clock signals.

Clock Generation

The PXIe-6674 includes built-in advanced clock generation circuitry for generating clock signals below 1 Hz to 1 GHz with very fine frequency resolution. The clock generation circuitry is based on a direct digital synthesis (DDS) with an 800 MHz reference phase locked to PXIe_CLK100. This allows the DDS to generate a 150 MHz to 300 MHz signal with microhertz resolution. The output from the DDS can then be divided down to lower frequencies, used directly, or multiplied up using a phase locked voltage controlled oscillator.

The individual components which make up the clock generation circuitry are controlled by NI-Sync software, which allows the user to simply specify the frequency they wish the clock generation circuitry to produce. NI-Sync will then configure the clock generation circuitry to give the closest possible frequency match to the requested frequency and do so with the configuration that gives the lowest possible phase noise. The user may request a clock frequency up to 1 GHz (frequencies beyond 1 GHz are possible but performance is not specified). The precision of the frequency generated is that of the DDS scaled up or down for any division or multiplication done to generate the requested frequency, as shown in *Table 4.* on page 13.

Table 4. Resolution by Frequency Ranges

Clock Generation Frequency	Resolution
18.75 MHz to 37.5 MHz	0.355 ΩHz
37.5 MHz to 75 MHz	0.711 ΩHz
75 MHz to 150 MHz	1.42 ΩHz
150 MHz to 300 MHz	2.84 ΩHz
300 MHz to 600 MHz	5.68 ΩHz
600 MHz to 1 GHz	11.4 ΩHz

ClkIn

CLKIN can be routed to the FPGA and used as a trigger synchronization clock inside the FPGA.

Because the PXIe-6674 is not designed for use in the system timing slot, it can not drive CLKIN to PXI_CLK10_IN for overdriving PXI_CLK10 and PXIe_CLK100. The PXIe-6674T is required for this functionality.

PXIe_DSTARA, PXIe_DSTARB, and PXIe_DSTARC

The PXI Express architecture includes a set of three high speed differential signal paths to connect the system timing slot to each PXI Express peripheral slot (up to 17 peripheral slots). These signals are PXIe_DSTARA, PXIe_DSTARB, and PXIe_DSTARC.

- PXIe_DSTARA—PXIe_DSTARA is used to send clock signals from the system timing slot to each PXI Express peripheral slot in a star configuration. PXIe_DSTARA uses LVPECL signaling and closely matched trace lengths to achieve low skew, high speed clock routing capabilities. The PXIe-6674 can route its DSTARA to CLKOUT and PFI_LVDS.
- PXIe_DSTARB—PXIe_DSTARB is used to send trigger signals from the system timing slot to each PXI Express peripheral slot in a star configuration. PXIe_DSTARB uses LVDS signaling and closely matched trace lengths to achieve faster, more precise triggering than is achievable with PXI_STAR or PXI_TRIG.
- PXIe_DSTARC—PXIe_DSTARC is used to send trigger signals from each PXI Express peripheral slot to the system timing slot in a star configuration. PXIe_DSTARC uses LVDS signaling and closely matched trace lengths and can be used to send a trigger signal or clock signal to the system timing module.

PFI_LVDS<0..2>

To allow for sending and receiving signals between system timing modules that are too fast for single ended PFI signaling, two PFI SMA connectors can be combined to send or receive LVDS signals. *Table 5.* on page 14 shows the relation between the front panel SMA connectors used for PFI and PFI_LVDS.

Table 5. Combinations of PFI Lines for PFI_LVDS

PFI Lines	PFI_LVDS Lines
PFI 0	PFI_LVDS 0 Negative
PFI 1	PFI_LVDS 0 Positive
PFI 2	PFI_LVDS 1 Negative
PFI 3	PFI_LVDS 1 Positive
PFI 4	PFI_LVDS 2 Negative
PFI 5	PFI_LVDS 2 Positive

Each of the three PFI_LVDS can be enabled for LVDS operation or used for two single ended PFIs. When enabled for LVDS operation, the PFI_LVDS pair can be configured as either an input or an output. PFI_LVDS lines can not be used as an input and output at the same time.

Because of the increased speed capabilities, the PFI_LVDS include additional routing capabilities not offered with the single ended PFI. When used as an input, the PFI_LVDS signal goes to the FPGA for trigger routing. When used as an output, the PFI_LVDS can be sourced from the FPGA for trigger usage, or from either the PXI_DSTARA or high speed CLKOUT outputs.

If the PFI_LVDS output is used for trigger routing, it is sourced from the FPGA and has all the same trigger routing characteristics as other trigger destinations. Refer to the *Using the Front Panel PFIs for LVDS Triggers* section for details on using PFI_LVDS for sending and receiving trigger signals.

CLKOUT

The CLKOUT SMA connector on the front panel provides a means to export a clock signal from the PXIe-6674 to an external device or another system timing module. The CLKOUT driver uses two separate circuits for driving CLKOUT, one for low speed frequencies (50 MHz and below) and one for high speed (above 50 MHz). The low speed driver uses 5 V CMOS logic with source impedance of 50 Ω and is AC coupled. The high speed driver produces an 800 mv_{pp} swing into a 50 Ω load and is also AC coupled.

The sources available to be routed to CLKOUT differ depending on whether the low speed or high speed driver is used. The sources available to the low speed driver are PXI_CLK10 and Clock Generation for generated frequencies 50 MHz and below. Sources available to the high speed CLKOUT are Clock Generation and PXIe_DSTARA.

NI-Sync software will select the low speed or high speed driver automatically based on the source connected to CLKOUT.

Routing Trigger Signals

The PXIe-6674 has versatile trigger routing capabilities. It can route signals to and from the front panel, the PXI_STAR trigger, the PXI_TRIG triggers, and PXIe_DSTARB/ PXIe_DSTARC.

Figure 4. on page 15 and *Figure 5.* on page 16 summarize the routing features of the PXIe-6674. The remainder of this chapter details the capabilities and constraints of the routing architecture.

Figure 4. High-Level Schematic of PXIe-6674 Signal Routing Architecture

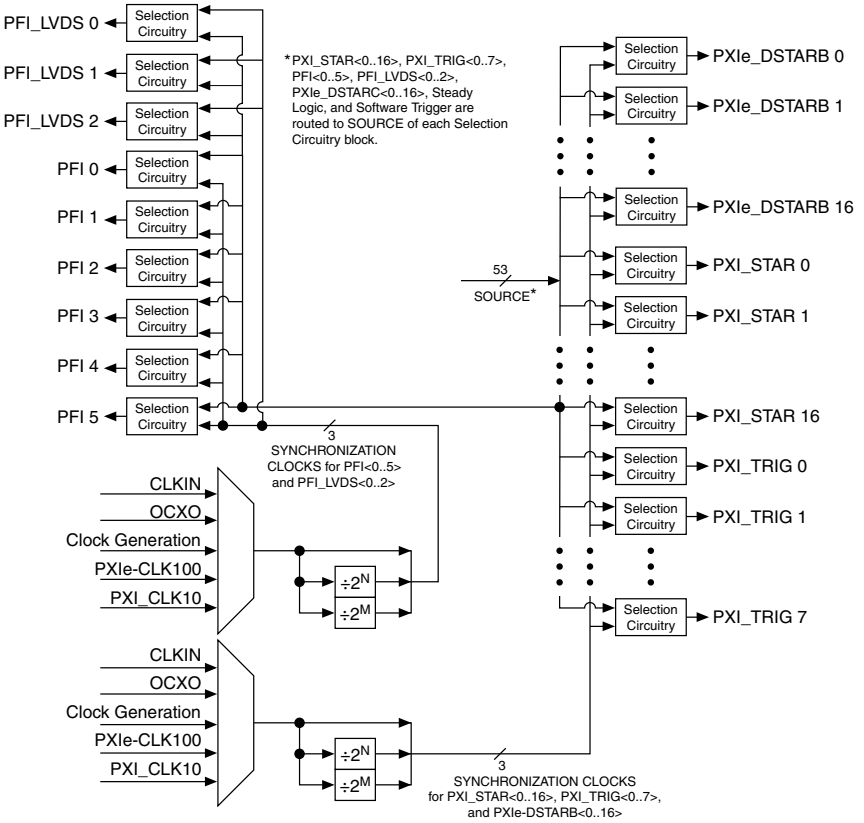
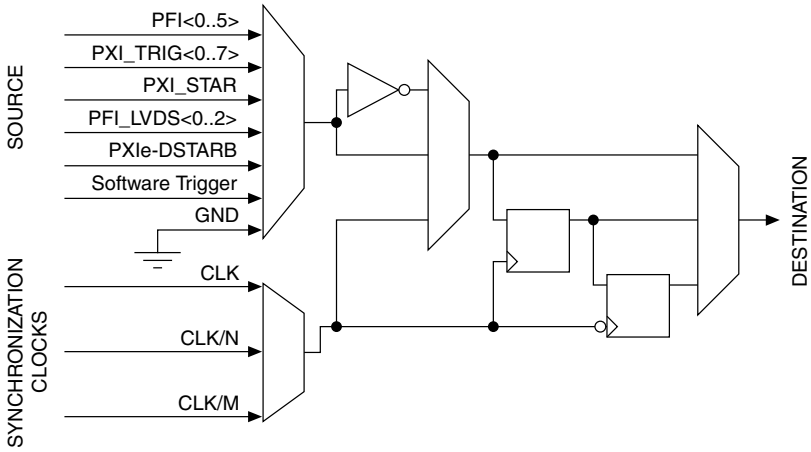


Figure 5. on page 16 provides a more detailed view of the selection circuitry referenced in *Figure 4.* on page 15.

Figure 5. Signal Selection Circuitry Diagram



Determining Sources and Destinations

All signal routing operations can be characterized by a *source* (input) and a *destination*. In addition, synchronous routing operations must also define a third signal known as the *synchronization clock*. Refer to the *Choosing the Type of Routing* section for more information on synchronous routing versus asynchronous routing.

Figure 6. on page 17 summarizes the sources and destinations of the PXIe-6674.

Figure 6. Sources and Destinations for PXIe-6674 Signal Routing Operations

			Destinations					
				Front Panel		Backplane		
			CLKOUT	PFI <0..5>	PFI_LVDS <0..2>	PXI_STAR Peripheral	PXI_TRIG <0..7>	DSTARC Peripheral
Sources	Front Panel	CLKIN	✓	✓†	✓†	✓†	✓†	✓†
		PFI<0..5>		✓	✓	✓	✓	✓
		PFI_LVDS <0..2>		✓	✓	✓	✓	✓
	Backplane	PXI_ CLK10	✓	✓†	✓†	✓†	✓†	✓†
		PXI_ CLK100		✓†	✓†	✓†	✓†	✓†
		PXI_STAR Peripheral		✓	✓	✓	✓	✓
		PXI_TRIG <0..7>		✓	✓	✓	✓	✓
		DSTARA Peripheral	✓		✓			
		DSTARB Peripheral		✓	✓	✓	✓	✓
	Onboard	Clk Gen	✓	✓†	✓	✓†	✓†	✓†
		Global Software		✓	✓	✓	✓	✓

† Routing PXI_CLK10, PXIe_CLK100, or ClkGen is accomplished by setting the synchronization clock (NI-Sync Property Node) to the desired clock source and then routing the synchronization clock as the source.

	Route made through the FPGA.
	Route to PFI_LVDS can be made through the FPGA when used as a trigger, or through the PXIe-DTARA network when used as a clock.

Using Front Panel PFIs as Single Ended Inputs

The front-panel PFIs can receive external signals from 0 to +5 V. They can be terminated programmatically with 50 Ω resistances to match the cable impedance and minimize reflections.

Note Terminating the signals with a 50 Ω resistance is recommended when the source is another PXIe-6674 or any other source with a 50 Ω output.

The voltage thresholds for the front-panel PFI inputs are programmable. The input signal is generated by comparing the input voltage on the PFI connectors to the voltage output of software-programmable DACs. The thresholds for the PFI lines are individually

programmable, which is useful if you are importing signals from multiple sources with different voltage swings.

Using Front Panel PFIs as Single Ended Outputs

The front panel PFI outputs are +3.3 V drivers with 50 Ω output impedance. The outputs can drive 50 Ω loads, such as a 50 Ω coaxial cable with a 50 Ω receiver. This cable configuration is the recommended setup to minimize reflections. With this configuration, the receiver sees a single +1.6 V step—a +3.3 V step split across the 50 Ω resistors at the source and the destination.

You also can drive a 50 Ω cable with a high-impedance load. The destination sees a single step to +3.3 V, but the source sees a reflection. This cable configuration is acceptable for low-frequency signals or short cables.

You can independently select the output signal source for each of the PFI lines from one of the following sources:

- Another PFI<0..5>
- Another PFI pair in LVDS mode
- PXI_TRIG<0..7>
- PXI_STAR
- Global software trigger
- PFI synchronization clock
- PXIe_DSTARB
- Steady logic high or low

The PFI synchronization clock may be any of the following signals:

- Clock Generation
- PXI_CLK10
- PXIe_CLK100
- CLKIN
- Any of the previously listed signals divided by the first frequency divider (2^n, up to 512).
- Any of the previously listed signals divided by the second frequency divider (2^m, up to 512)

Refer to the *Choosing the Type of Routing* section for more information on the synchronization clock.

Note The PFI synchronization clock is the same for all routing operations in which PFI<0..5> or PFI_LVDS<0..2> is defined as the output, although the divide-down ratio for this clock (full rate, first divider, second divider) may be chosen on a per route basis.

Using Front Panel PFIs for LVDS Triggers

To allow for sending and receiving signals between system timing modules that are too fast for single ended PFI signaling, two PFI SMA connectors can be combined to send or receive LVDS signals. *Table 5.* on page 14 shows the relation between the front panel SMA connectors used for PFI and PFI_LVDS.

When used for trigger routing, the PFI_LVDS signals are routed to and from the FPGA. You can independently select the output signal source for each PFI_LVDS line from one of the following sources:

- Another PFI<0..5>
- Another PFI pair in LVDS mode
- PXI_TRIG<0..7>
- PXI_STAR
- Global software trigger
- PFI synchronization clock
- PXIe_DSTARB
- Steady logic high or low

The PFI synchronization clock is also used for the PFI_LVDS and may be one of the following signals:

- Clock Generation
- PXI_CLK10
- PXIe_CLK100
- CLKIN
- Any of the previously listed signals divided by the first frequency divider (2^n, up to 512)
- Any of the previously listed signals divided by the second frequency divider (2^m, up to 512).

Refer to the *Choosing the Type of Routing* section for more information on the synchronization clock.

Note The PFI synchronization clock is the same for all routing operations in which PFI<0..5> or PFI_LVDS<0..2> is defined as the output, although the divide-down ratio for this clock (full rate, first divider, second divider) may be chosen on a per route basis.

Using the PXI Triggers

The PXI triggers go to all the slots in the chassis. All modules receive the same PXI triggers, so PXI trigger 0 is the same for the system timing slot as it is for Slot 3, and so on. This feature makes the PXI triggers convenient in situations where you want, for instance, to start an acquisition on several devices at the same time because all modules will receive the same trigger.

The frequency on the PXI triggers should not exceed 5 MHz to preserve signal integrity. The signals do not reach each slot at precisely the same time. A difference of several nanoseconds between slots can occur in an eight-slot chassis. However, this delay is not a problem for many applications.

You can independently select the output signal source for each PXI trigger line from one of the following sources:

- PFI<0..5>
- PFI_LVDS<0..2>
- PXI_TRIG<0..7>
- PXI_STAR
- Global software trigger
- Backplane synchronization clock
- PXIe_DSTARB
- Steady logic high or low.

The backplane synchronization clock may be any of the following signals:

- Clock Generation
- PXI_CLK10
- PXIe_CLK100
- CLKIN
- Any of the previously listed signals divided by the first frequency divider (2^n, up to 512)
- Any of the previously listed signals divided by the second frequency divider (2^m, up to 512)

Refer to the *Choosing the Type of Routing* section for more information about the synchronization clock.

Note The backplane synchronization clock is the same for all routing operations in which PXI_TRIG<0..7>, PXIe_DSTARC, or PXI_STAR is defined as the output, although the divide-down ratio for this clock (full rate, first divider, second divider) may be chosen on a per route basis.

Using the PXI Star Trigger

There are up to 17 PXI star triggers per chassis. Each trigger line is a dedicated connection between the system timing slot and one other slot. The PXI Specification, Revision 2.1, requires that the propagation delay along each star trigger line be matched to within 1 ns. A typical upper limit for the skew in most NI PXI Express chassis is 500 ps. The low skew of the PXI star trigger bus is useful for applications that require triggers to arrive at several modules nearly simultaneously.

The star trigger lines are bidirectional, so signals can be sent to the system timing slot from a module in another slot or from the system timing slot to the other module.

You can independently select the output signal source for the PXI star trigger line from one of the following sources:

- PFI<0..5>
- PFI_LVDS<0..2>
- PXI_TRIG<0..7>
- Global software trigger
- Backplane synchronization clock
- PXIe_DSTARB
- Steady logic high or low

Refer to the *Using the PXI Triggers* section for more information on the backplane synchronization clock.

Using the PXIe_DSTARB and PXIe_DSTARC Triggers

To improve beyond the performance the PXI Star triggers offer in low skew trigger routing, PXI Express implements PXIe_DSTARB and PXIe_DSTARC triggers. Each PXI Express peripheral slot in a PXI Express chassis has independent PXIe_DSTARB and PXIe_DSTARC connections with the system timing slot module. This allows peripheral modules to send triggers to the system timing module using PXIe_DSTARC and for the system timing module to send triggers to peripheral modules using PXIe_DSTARB. Both PXIe_DSTARB and PXIe_DSTARC are one directional. The PXI Express Specification requires PXI Express chassis to limit the skew between any two PXIe_DSTAR routes to 150 ps.

The PXIe-6674 receives PXIe_DSTARB and can route it as a trigger source. The PXIe-6674 can independently select from the following sources to be routed to PXIe_DSTARC:

- PFI<0..5>
- PFI_LVDS<0..2>
- PXI_TRIG<0..7>
- PXI Star Trigger
- PXIe_DSTARB
- Global Software Trigger
- Steady logic high or low
- Backplane synchronization clock.

Refer to the *Using the PXI Triggers* section for more information on the backplane synchronization clock.

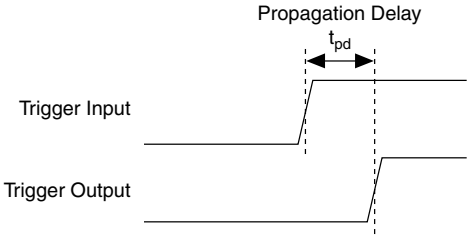
Choosing the Type of Routing

The PXIe-6674 routes signals in one of two ways: asynchronously or synchronously. The following sections describe the two routing types and the considerations for choosing each type.

Asynchronous routing is the most straightforward method of routing signals. Any asynchronous route can be defined in terms of two signals: a *source* and a *destination*. A

digital pulse or train comes in on the source and is propagated to the destination. When the source signal goes from low to high, this rising edge is transferred to the destination after a propagation delay through the module. *Figure 7.* on page 22 illustrates an asynchronous routing operation.

Figure 7. Asynchronous Routing Operation



Some delay is always associated with an asynchronous route, and this delay varies among PXIe-6674 modules, depending on variations in temperature and chassis voltage. Typical delay times in the PXIe-6674 for asynchronous routes between various sources and destinations are given in the device's Specifications.

Asynchronous routing works well if the total system delays are not too long for the application. Propagation delay could be caused by the following reasons.

- Output delay on the source.
- Propagation delay of the signal across the backplane(s) and cable(s).
- Propagation delay of the signal through the PXIe-6674.
- Time for the receiver to recognize the signal.

Both the source and the destination of an asynchronous routing operation on the PXIe-6674 can be any of the following lines:

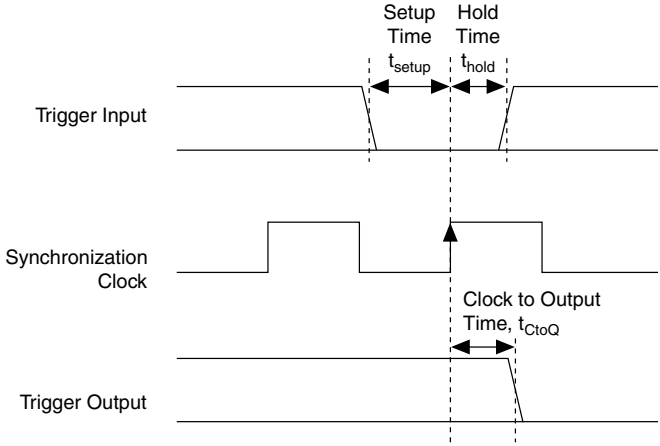
- Any front panel PFI pin (PFI<0..5>) as single ended.
- Any front panel PFI pin as LVDS (PFI_LVDS<0..2>)
- Any PXI star trigger line (PXI_STAR<0..16>)
- Any PXI trigger line (PXI_TRIG<0..7>)
- Any PXIe_DSTARB<0..16>

Synchronous Routing

A synchronous routing operation is defined in terms of three signals: a *source*, a *destination*, and a *synchronization clock*. Unlike asynchronous routing, the output of a synchronous routing operation does not directly follow the input after a propagation delay. Instead, the logic state of the input is sampled on each active edge of the synchronization clock, and the output is set to that logic state after a small delay, as shown in *Figure 8.* on page 23.

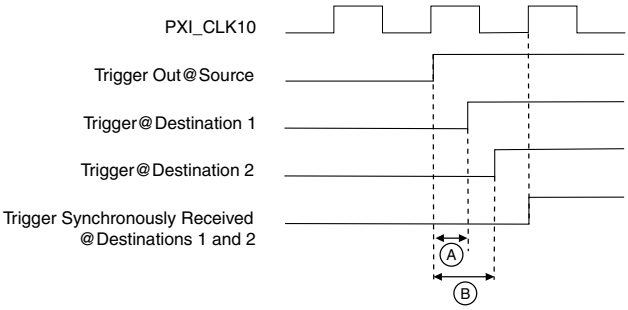
Figure 8. on page 23 shows a timing diagram that illustrates synchronous routing.

Figure 8. Synchronous Routing Operation



The PXIe-6674 board supports synchronous routing to either the rising or falling edge of the synchronization clock. In addition, the polarity of the destination signal can be inverted, which is useful when handling active-low digital signals. Synchronous routing can be useful for eliminating skew when sending triggers to several destinations. For example, when sending triggers using the PXI Trigger lines, the trigger arrives at each slot at a slightly different time. However, if the trigger is sent and received synchronously using a low-skew synchronization clock (for example, PXI_CLK10), all receiving devices can act on the trigger at the same time, as shown in *Figure 9.* on page 23:

Figure 9. Synchronous Routing to Multiple Destinations



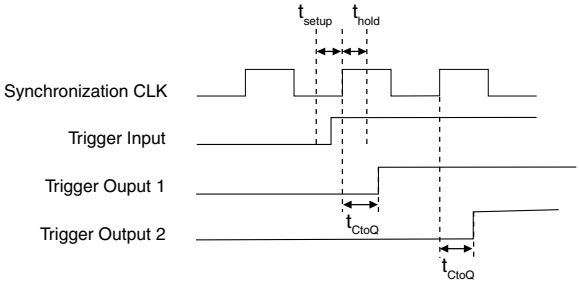
A: Propagation delay from source to destination 1.

B: Propagation delay from source to destination 2.

Synchronous routing requires the input to be stable at a logic low or logic high state with a window of time around the clock edge. This window of time around the clock edge is defined by the setup time (t_{setup}) and hold time (t_{hold}). If the input signal changes within this window of

time, it is undetermined whether the output of the synchronous route will go to the old or new logic state. This is important, for example, if a source is being routed synchronously to several destinations. If the source signal changes within the setup-and-hold window around the synchronization clock dge, one of the destinations might go to the new logic level while the other destination might remain at the old logic level and change when the next synchronization clock edge occurs, as shown in *Figure 10.* on page 24

Figure 10. Synchronous Routing Uncertainty with Setup-and-Hold Variations



Therefore, if your application requires that the trigger arrive at the multiple destinations simultaneously, you must ensure that the input is table within the setup and hold window around the synchronization clock edge. For more information and possible methods to ensure this requirement is met, go to `ni.com/info` and enter the Info Code `SyncTriggerRouting`.

Possible sources for synchronous routing with the PXIe-6674 include the following sources:

- Any front panel PFI pin as single ended.
- Any front panel PFI pin as LVDS.
- Any PXI star trigger line (PXI_STAR<0..16>)
- Any PXI trigger line (PXI_TRIG<0..7>)
- Any PXIe_DSTARC<0..16>
- Global software trigger
- The synchronization clock itself.

They synchronization clock for a synchronous route can be any of the following signals.

- 10 MHz PXI_CLK10
- 100 MHz PXIe_CLK100
- Clock Generation
- OCXO
- CLKIN
- One of two "divided copies" of any of the previously listed five signals. The PXIe-6674T includes two clock divider circuits that can divide the synchronization clock signals by any power of 2 up to 512.

Refer to *Figure 4.* on page 15 and *Figure 5.* on page 16 for an illustration of how the PXIe-6674 performs synchronous routing operations.

Calibration

This chapter discusses the calibration of the PXIe-6674.

Calibration consists of verifying the measurement accuracy of a device and correcting for any measurement error. The PXIe-6674 is factory calibrated before shipment at approximately 25 °C to the levels indicated in the device's specifications. The associated calibration constants—the corrections that were needed to meet specifications—are stored in the onboard non-volatile memory (EEPROM). The driver software uses these stored values.

Factory Calibration

The factory calibration of the PXIe-6674 involves calculating and storing four calibration constants. These values control the accuracy of two features of the device, which are discussed in the following sections.

OXCO Frequency

The OCXO frequency can be varied over a small range. The output frequency of the OCXO is adjusted using this constant to meet the specification listed in the PXIe-6674 Specifications.

PXI_CLK10 Phase

When using the PLL to lock PXI_CLK10 to an external reference clock, the phase between the clocks can be adjusted. The time between rising edges of PXI_CLK10 and the input clock is minimized using this constant.

Note The PXI_CLK10 phase is set during manufacturing and does not need to be recalibrated.

Compliance

Electromagnetic Compatibility Information

This hardware has been tested and found to comply with the regulatory requirements and limits for electromagnetic compatibility (EMC) as indicated in the hardware's Declaration of Conformity (DoC).

[4] The Declaration of Conformity (DoC) contains important EMC compliance information and instructions for the user and installer. To obtain the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

If this hardware does cause interference with licensed radio communications services or other nearby electronics, which can be determined by turning the hardware off and on, you are encouraged to try to correct the interference by one or more of the following measures:

- Reorient the antenna of the receiver (the device suffering interference).
- Relocate the transmitter (the device generating interference) with respect to the receiver.
- Plug the transmitter into a different outlet so that the transmitter and the receiver are on different branch circuits.

Some hardware may require the use of a metal, shielded enclosure (windowless version) to meet the EMC requirements for special EMC environments such as for marine use or in heavy industrial areas. Refer to the hardware's user documentation and the DoC[4] for product installation requirements.

When the hardware is connected to a test object or to test leads, the system may become more sensitive to disturbances or may cause interference in the local electromagnetic environment.

Operation of this hardware in a residential area is likely to cause harmful interference. Users are required to correct the interference at their own expense or cease operation of the hardware.

Changes or modifications not expressly approved by National Instruments could void the user's right to operate the hardware under the local regulatory rules.

Caution To ensure the specified EMC performance, operate this product only with double-shielded cables (such as RG-223 double-shielded cables) and accessories.

Caution To ensure the specified EMC performance, you must install PXI EMC filler panels, National Instruments part number 778700-01, in all open chassis slots.

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